1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEMATIC,CORNHOLIO

5/12/2009

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

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1	1	Table of Contents	N/A N/A
2	2	System Block Diagram	N/A N/A
3	3	Power Block Diagram	03/13/2008 DRAGON
4	4	BOM Configuration	N/A N/A
5	5	Revision History	N/A N/A
6	7	Functional / ICT Test	N/A N/A
7	8	Power Aliases	N/A N/A
8	9	Signal Aliases	01/13/2009 WFERRY_K19I
9	10	CPU FSB	02/05/2009 K24_MLB
10	11	CPU Power & Ground	02/05/2009 K24_MLB
11	12	CPU Decoupling	02/05/2009 K24_MLB
12	13	eXtended Debug Port(MiniXDP)	02/05/2009 K19_MLB
13	14	MCP CPU Interface	02/05/2009 T18_MLB
14	15	MCP Memory Interface	02/05/2009 T18_MLB
15	16	MCP Memory Misc	02/05/2009 T18_MLB
16	17	MCP PCIe Interfaces	02/05/2009 T18_MLB
17	18	MCP Ethernet & Graphics	02/05/2009 T18_MLB
18	19	MCP PCI & LPC	02/05/2009 T18_MLB
19	20	MCP SATA & USB	02/05/2009 T18_MLB
20	21	MCP HDA & MISC	02/05/2009 T18_MLB
21	22	MCP Power & Ground	02/05/2009 T18_MLB
22	25	MCP Standard Decoupling	02/05/2009 T18_MLB
23	26	MCP Graphics Support	02/05/2009 K19_MLB
24	28	SB Misc	01/06/2009 WFERRY_K19I
25	29	FSB/DDR3 Vref Margining	02/05/2009 K24_MLB
26	31	DDR3 SO-DIMM Connector A	02/05/2009 K19_MLB
27	32	DDR3 SO-DIMM Connector B	02/05/2009 K19_MLB
28	33	DDR3 Support	02/05/2009 T18_MLB
29	34	Right Clutch Connector	03/04/2009 K19_MLB
30	35	SECUREDIGITAL CARD READER	03/23/2009 K19_MLB
31	37	Ethernet PHY (RTL8211CL)	02/05/2009 (K19I_MLB)
32	38	Ethernet & AirPort Support	02/05/2009 K19_MLB
33	39	Ethernet Connector	03/13/2009 K19_MLB
34	41	FireWire LLC/PHY (FW643E)	02/05/2009 T18_MLB
35	42	FireWire Port Power	03/18/2009 K19_MLB
36	43	FireWire Ports	02/05/2009 K19_MLB
37	45	SATA Connectors	03/23/2009 K19_MLB
38	46	External USB Connectors	02/05/2009 K19_MLB
39	48	Front Flex Support	02/05/2009 K19_MLB
40	49	SMC	02/05/2009 T18_MLB
41	50	SMC Support	(11/25/2008) (K19_MLB)
42	51	LPC+SPI Debug Connector	02/05/2009 K19_MLB
43	52	K19i SMBus Connections	12/12/2008 WFERRY_K19I
44	53	VOLTAGE SENSING	02/05/2009 K24_MLB
45	54	Current Sensing	12/16/2008 WFERRY_K19I
46	55	Thermal Sensors	02/05/2009 K24_MLB
47	56	Fan	02/05/2009 K24_MLB
48	57	WELLSPRING 1	02/05/2009 K24_MLB
49	58	WELLSPRING 2	02/25/2009 K24_MLB
50	59	Sudden Motion Sensor (SMS)	02/05/2009 K19_MLB
51	60	DEBUG SENSORS AND ADC	03/25/2009 K19_MLB
52	61	SPI ROM	02/05/2009 K19_MLB
53	62	AUDIO: CODEC/REGULATOR	03/17/2009 K19_MLB
54	63	AUDIO: LINE INPUT FILTER	03/02/2009 K19_MLB
55	65	AUDIO: HEADPHONE FILTER	02/05/2009 K19_MLB
56	66	AUDIO:SPEAKER AMP	02/05/2009 K19_MLB
57	67	AUDIO: JACKS	03/20/2009 CASEYHARDY_K19
58	68	AUDIO: JACK TRANSLATORS	03/17/2009 K19_MLB
59	69	DC-In & Battery Connectors	03/18/2009 K19_MLB
60	70	PBus Supply & Battery Charger	03/18/2009 K19_MLB
61	71	IMVP6 CPU VCore Regulator	02/05/2009 K19_MLB
62	72	5V / 3.3V Power Supply	01/13/2009 WFERRY_K19I
63	73	1.5V DDR3 Supply	02/04/2009 K19_MLB
64	75	MCP CORE REGULATOR	02/03/2009 K19_MLB
65	76	CPU VTT Power Supply	(12/05/2008) (K19_MLB)
66	77	MISC POWER SUPPLIES	02/25/2009 K24_MLB
67	78	POWER SEQUENCING	02/05/2009 K24_MLB
68	79	POWER FETS	03/12/2009 K24_MLB
69	90	LVDS Display Connector	02/05/2009 K19_MLB
70	93	DISPLAYPORT SUPPORT	12/19/2008 K24_MLB
71	94	DisplayPort Connector	02/05/2009 K19_MLB
72	97	LCD BACKLIGHT DRIVER	02/10/2009 K19_MLB
73	98	LCD Backlight Support	03/16/2009 K24_MLB
74	99	LCD Backlight Driver (MC34845)	02/09/2009 VEMURI_K19I
75	100	CPU/FSB Constraints	02/05/2009 T18_MLB
76	101	Memory Constraints	02/05/2009 T18_MLB
77	102	MCP Constraints 1	02/05/2009 T18_MLB
78	103	MCP Constraints 2	02/05/2009 T18_MLB
79	104	Ethernet Constraints	02/05/2009 T18_MLB
80	105	FireWire Constraints	02/05/2009 T18_MLB
81	106	SMC Constraints	02/05/2009 T18_MLB
82	108	K19i Specific Constraints	01/08/2009 WFERRY_K19I
83	109	K19i PCB Rule Definitions	12/12/2008 WFERRY_K19I

Integration Issues to be Resolved

JTAG_MCP_TDO (IN, MAKE_BASE=TRUE) = JTAG_MCP_TDO (OUT)
XDP_TDO (IN, MAKE_BASE=TRUE) = XDP_TDO (OUT)
(Should rename J1300 nets now that JTAG level-shifter is gone)

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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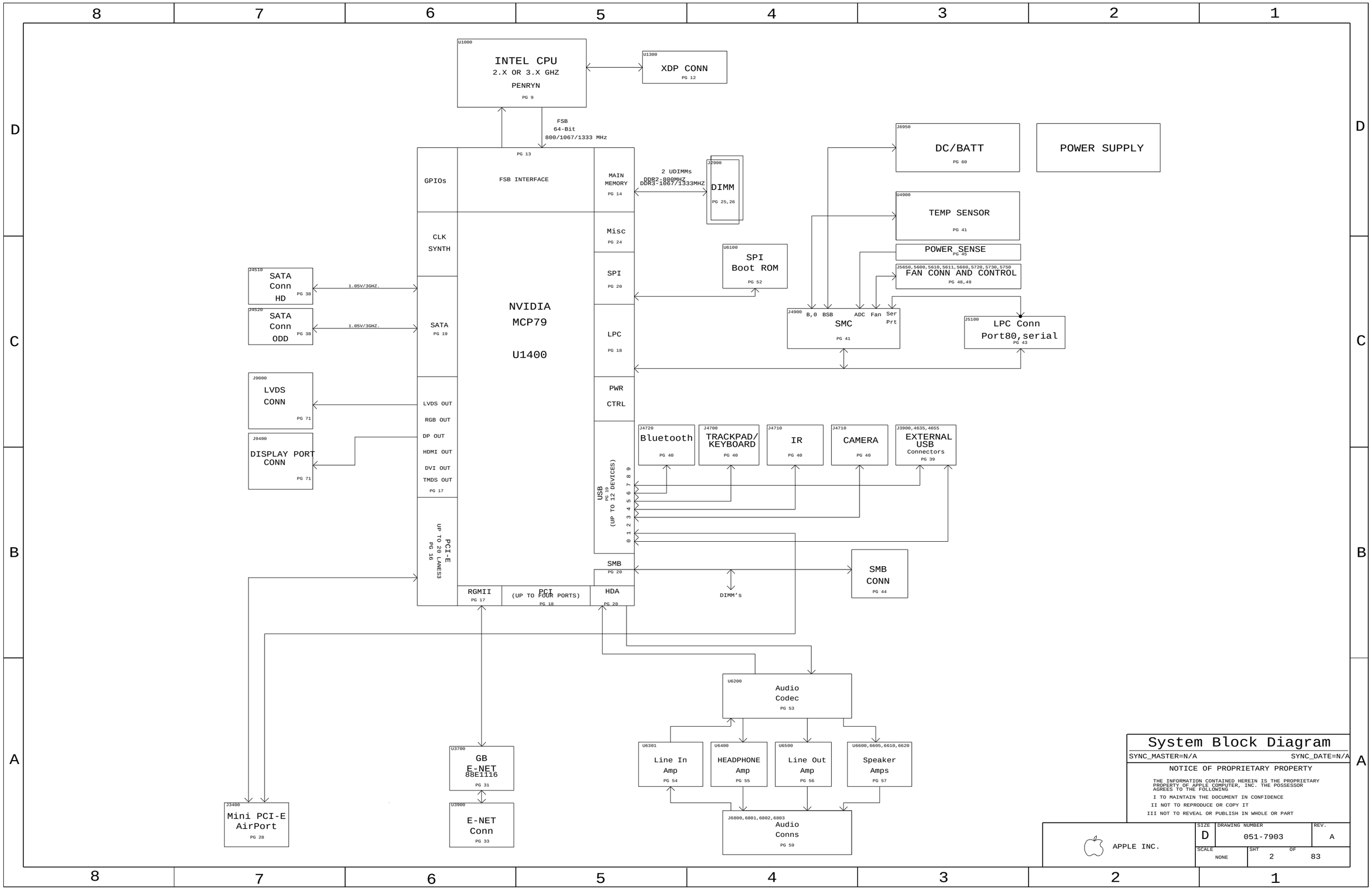
TITLE

DRAWING NUMBER 051-7903 REV. A

SHT 1 OF 83



System Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A

SCALE	SHT	OF
NONE	2	83

POWER SYSTEM ARCHITECTURE

D6905
D6905
PPVIN_G3H_P3V42G3H
PBUS_VSENSE
Q5315
ENABLE
3.425V G3HOT
LT3470
U6990
VOUT
PP3V42_G3H_REG
SMC PWRGD
RN5VD30A-F
U5000
7A FUSE
PPVBAT_G3H_CHGR_REG
PPBUS_G3H
CPUVTTS0_EN
(S0)
EN_PSV
CPUVTT
(1.05V)
TPS51117
U7600
VOUT
PGOOD
PPCPUVTT_S0_REG_R
(8A MAX CURRENT)
R5492
PPCPUVTT_S0
CPUVTTS0_PGOOD
AC
ADAPTER
IN
DCIN(16.5V)
6A FUSE
U7970
CHGR_EN
(S5)
ENABLES
VIN
VOUT
PBUS SUPPLY/
BATTERY CHARGER
ISL6258A
U7000
SMC_DCIN_ISENSE
U5403
SMC_BATT_ISENSE
J6950
3S2P
(9 TO 12.6V)
BATT_POS_F
Q7050
CHGR_BGATE
PPVBAT_G3H_CHGR_OUT
U5480
SMC_CPU_VSENSE
SMC_CPU_ISENSE
CPU VCORE
ISL9504B
VIN
VOUT
VR_ON
PGOOD
U7400
IMVP_VR_ON
PPVCORE_CPU_S0_REG
(44A MAX CURRENT)
VR_PWRGOOD_DELAY
P1V05S0_EN
1.05V S0
FETS
(Q7951 TO Q7953)
PP1V05_S0_FET
PPBUS_G3H
MCP79
PWRBTN*
PLTRST*
RSMRST*
LPC_RESET_L
MCP_PS_PWRGD
PS_PWRGD
CPUPWRGD(GPIO49)
CPU_PWRGD
U2850
U1400
CPU_RESET#
FSB_CPURST_L
CPU
PWRGOOD
RESET*
U1000
4.6V AUDIO
MAX8902A
U6201
VIN
EN
VOUT
PP4V6_AUDIO_ANALOG
MCP79
PM_SLP_S4_L
SLP_S3#
U1400
PCI_RESET0#
P3V3S3_EN
DDRREG_EN
P5VLTS3_EN
RC DELAY
SMC
U4900
P16
P60
SMC_PM_G2_EN
(S5)
P1V05_S5_EN
RC DELAY
1.05V (S5)
TPS62510
U7750
VOUT
PP1V05_S5_REG
P5VRTS0_EN_L
P3V3S5_EN_L
VIN
EN1
EN2
5V
(RT)
3.3V
TPS51125
U7200
VOUT1
VOUT2
PGOOD1,2
VREG3
PP5VRT_S0_REG
(4A MAX CURRENT)
PP3V3_S5_REG
(4A MAX CURRENT)
P5V3V3_PGOOD
Q7800
Q7910
Q7930
Q3810
P3V3S3_EN
P3V3S0_EN
P3V3ENET_EN_L
PP5VRT_S0
PP3V3_S5
PP3V3_S3_FET
PP3V3_S0_FET
P3V3_ENET_FET
GOSHAWK6P
U9701
BKLT_EN
ENA
PPVOUT_S0_LCDBKLT
1.2V YUKON
U3850
ENETADD_EN
P1V2ENET_EN
RUN1
RUN2
LTC34074
PPVOUT_ENET_AVDD_REG
(0.8A MAX CURRENT)
PP1V2_ENET_REG
(0.8A MAX CURRENT)
Q3801
PM_SLP_S3_L
PM_ENET_EN_L
Q3802
WOL_EN
SMC_ADAPTER_EN
SMC
RSMRST_OUT(P15)
PWRGD(P12)→99ms DLY→
IMVP_VR_ON(P16)
RSMRST_IN(P13)
PWR_BUTTON(P90)
P17(BTN_OUT)
RST*
PM_RSMRST_L
IMVP_VR_ON
PLT_RST*
PM_PWRBTN_L
SMC_RESET_L
ALL_SYS_PWRGD
RSMRST_PWRGD
SMC_ONOFF_L
SLP_S5_L(P95)
SLP_S4_L(P94)
SLP_S3_L(P93)
U4900
SLP_S5_L
SLP_S4_L
SLP_S3_L
P5V3V3_PGOOD
MCPCORES0_PGOOD
CPUVTTS0_PGOOD
P5V_LT_S3_PGOOD
S0PGOOD_PWROK
=DDRREG_EN
=DDTVTT_EN
1.5V
S5
S3 0.75V
TPS51116
U7300
S3 TO S0
FETS
(Q7901 & Q7971)
PP1V5_S0_FET
R5491
PP1V5_S0
PP1V5_S3_REG
(12A MAX CURRENT)
PP0V75_S0_REG
(1A MAX CURRENT)
1.8V LDO
TPS79918DRV
U7760
PP1V8_S0_REG
PP3V3_S0
PP1V5_S0
PP1V05_S0
V1
V2
V3
LTC2909
U7870
RST*
P1V8S0_EN
MCPDDR_EN
CPUVTTS0_EN
MCPCORES0_EN
P1V05S0_EN
(S0)
P3V3S0_EN
(S0)
PBUSVSENS_EN
(S0)
P5VRTS0_EN_L
(S0)
MCP_CORE
5V (LT)
ISL6236
U7500
MCPCORES0_EN
P5VLTS3_EN
PPVCORE_S0_MCP_REG_R
(25A MAX CURRENT)
R5490
PPVCORE_S0_MCP
PP5VLT_S3_REG
(7A MAX CURRENT)
PP5VLT_S3

Power Block Diagram

SYNC_MASTER=DRAGON
SYNC_DATE=03/13/2008

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SCALE: NONE	SHT 3 OF 83	

BOM Variant

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9977	PCBA,CORNHOLIO,MLB,K19I	K19_COMMON,CPU_2_53GHZ,EEE_6Z9
085-0737	K19I MLB DEVELOPMENT	K19_DEVEL_PVT

BOM Groups

BOM GROUP	BOM OPTIONS
K19_COMMON	COMMON,ALTERNATE,K19_MCP,K19_MISC,K19_DEBUG_PVT,K19_PROGPARTS
K19_MCP	MCP_B03,BOOT_MODE_USER
K19_MISC	DP_ESD,EXTRACT_BUFF,ISL6258A,K19I,KB_BL,MIKEY,LDO_YES
K19_PROGPARTS	BOOTROM_PROG,SMC_PROG,IR_PROG,WELLSPRING_PROG
K19_DEVEL_ENG	BMON_ENG,DEBUG_ADC,XDP_CONN,LPCPLUS,VREFMRGN,BKLT_FS
K19_DEVEL_PVT	LPCPLUS
K19_DEBUG_ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K19_DEBUG_PVT	DEVEL_BOM,BMON_PROD,SMC_DEBUG_YES,XDP,NO_VREFMRGN
K19_DEBUG_PROD	BMON_PROD,SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3693	1	PDC,SLGE3,PRQ,2.00,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_0GHZ
337S3704	1	PDC,SLGE2,PRQ,2.26,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_26GHZ
337S3680	1	PDC,LGDZ,PRQ,2.40,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3640	1	PDC,SL3BX,PRQ,2.5,35W,1066,C0,6M,BGA	U1000	CRITICAL	CPU_2_5GHZ
337S3756	1	PDC,SLCFG,PRQ,2.53,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3641	1	PDC,SLB43,PRQ,2.8,35W,1066,C0,6M,BGA	U1000	CRITICAL	CPU_2_8GHZ
338S0710	1	IC,MCP79MXT-B3,35x35MM,BGA1437	U1400	CRITICAL	MCP_B03
338S0694	1	IC,RTL8251CA-VB-GR,GIGE TRANSCEIVER,48P	U3700	CRITICAL	
338S0654	1	IC-FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	

Programmable Parts

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC_BLANK
341S2460	1	IC,PRGRM,SMC EXTERNAL,K19I	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2458	1	IC,PRGRM,UNLOCK,K19I	U6100	CRITICAL	BOOTROM_PROG
338S0633	1	IC,CYPRS,CY7C63803-LQXC,4X4MM,USB,24-QFN	U4800	CRITICAL	IR_BLANK
341S2384	1	IR,ENCORE II,CY7C63803-LQXC	U4800	CRITICAL	IR_PROG
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
341S2503	1	IC,TP PSOC,M97,M98	U5701	CRITICAL	WELLSPRING_PROG

Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0737	1	K19I MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
152S0968	152S0966		ALL	Maglayer alt to Delta
128S0220	128S0262		ALL	KEMET alt to SANYO
152S0778	152S0693		ALL	CYNTEC AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
152S0694	152S0138		ALL	MAGLAYERS AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE

Bar Code Label / EEE

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6Z9]	CRITICAL	EEE_6Z9

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7903	1	SCHEM,CORNHOLIO,K19	SCH	CRITICAL	
820-2533	1	PCBF,MLB IG,K19	PCB	CRITICAL	

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A

SCALE	SHT	OF
NONE	4	83

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Revision History

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NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

Revision History

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A
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Functional Test Points

Fan Connectors

FUNC_TEST

TRUE	PP5V_S0	72 64 65 67 7 35 41 47 49 61 68 70	3 TPs
TRUE	FAN_RT_PWM	47	
TRUE	FAN_RT_TACH	47	
TRUE	GND		5 TPs

LVDS Connector

FUNC_TEST

TRUE	PP3V3_S0	58 61 66 67 68 69 71 72 82 35 37 41 43 45 46 47 48 53 57	
TRUE	PP3V3_SW_LCD	69	
TRUE	PPVOUT_S0_LCDBKLT	6 51 69 72 74	
TRUE	LVDS_DDC_CLK	8 17 69	
TRUE	LVDS_DDC_DATA	8 17 69	
TRUE	LVDS_CONN_A_DATA_N<0>	8 69	
TRUE	LVDS_CONN_A_DATA_P<0>	8 69	
TRUE	LVDS_CONN_A_DATA_N<1>	8 69	
TRUE	LVDS_CONN_A_DATA_P<1>	8 69	
TRUE	LVDS_CONN_A_DATA_N<2>	8 69	
TRUE	LVDS_CONN_A_DATA_P<2>	8 69	
TRUE	LVDS_CONN_A_CLK_F_N	69 82	
TRUE	LVDS_CONN_A_CLK_F_P	69 82	
TRUE	LVDS_CONN_B_DATA_N<0>	8 69	
TRUE	LVDS_CONN_B_DATA_P<0>	8 69	
TRUE	LVDS_CONN_B_DATA_N<1>	8 69	
TRUE	LVDS_CONN_B_DATA_P<1>	8 69	
TRUE	LVDS_CONN_B_DATA_N<2>	8 69	
TRUE	LVDS_CONN_B_DATA_P<2>	8 69	
TRUE	LVDS_CONN_B_CLK_F_N	69 82	
TRUE	LVDS_CONN_B_CLK_F_P	69 82	
TRUE	LED_RETURN_1	69 72 74	
TRUE	LED_RETURN_2	69 72 74	
TRUE	LED_RETURN_3	69 72 74	
TRUE	LED_RETURN_4	69 72 74	
TRUE	LED_RETURN_5	69 72 74	
TRUE	LED_RETURN_6	69 72 74	
TRUE	BKL_ISEN1	72	
TRUE	BKL_ISEN2	72	
TRUE	BKL_ISEN3	72	
TRUE	BKL_ISEN4	72	
TRUE	BKL_ISEN5	72	
TRUE	BKL_ISEN6	72	
TRUE	GND		5 TPs

IPD Flex Connector

FUNC_TEST

TRUE	PP3V3_S3_LDO	6 49	
TRUE	PP18V5_S3	6 49	
TRUE	Z2_CS_L	48 49	
TRUE	Z2_DEBUG3	48 49	
TRUE	Z2_MOSI	48 49	
TRUE	Z2_MISO	48 49	
TRUE	Z2_SCLK	48 49	
TRUE	Z2_BOOST_EN	49	
TRUE	Z2_HOST_INTN	48 49	
TRUE	Z2_CLKIN	48 49	
TRUE	Z2_KEY_ACT_L	48 49	
TRUE	Z2_RESET	48 49	
TRUE	PSOC_MISO	48 49	
TRUE	PSOC_MOSI	48 49	
TRUE	PSOC_SCLK	48 49	
TRUE	SMBUS_SMC_A_S3_SDA	6 29 40 43 49 81	
TRUE	SMBUS_SMC_A_S3_SCL	6 29 40 43 49 81	
TRUE	PSOC_F_CS_L	48 49	
TRUE	PICKB_L	48 49	
TRUE	GND		2 TPs

SD Card Connector

FUNC_TEST

TRUE	SD_D<7..0>	30 82	
TRUE	SD_CMD	30 82	
TRUE	SD_CLK	30 82	
TRUE	SD_CD_L	30	
TRUE	SD_WP	30	
TRUE	GND		2 TPs

Speaker Connectors

FUNC_TEST

TRUE	BI_MIC_LO	57 58	
TRUE	BI_MIC_SHIELD	57 58	
TRUE	BI_MIC_HI	57 58	
TRUE	SPKRCONN_L_OUT_P	56 57 82	
TRUE	SPKRCONN_L_OUT_N	56 57 82	
TRUE	SPKRCONN_R_OUT_P	56 57 82	
TRUE	SPKRCONN_R_OUT_N	56 57 82	
TRUE	SPKRCONN_S_OUT_P	56 57 82	
TRUE	SPKRCONN_S_OUT_N	56 57 82	
TRUE	GND		6 TPs

SATA ODD Connectors

FUNC_TEST

TRUE	PP5V_SW_ODD	6 37 51	4 TPs
TRUE	SMC_ODD_DETECT	37 40	
TRUE	SATA_ODD_R2D_P	37 77	
TRUE	SATA_ODD_R2D_N	37 77	
TRUE	SATA_ODD_D2R_C_N	37 77	
TRUE	SATA_ODD_D2R_C_P	37 77	
TRUE	GND		3 TPs

Keyboard Connector

FUNC_TEST

TRUE	PP3V3_S3	6 7 20 25 29 30 43 48 50 68	
TRUE	PP3V42_G3H	6 7 20 21 24 38 40 41 42 43 45 48 59 60 67	
TRUE	WS_KBD1	48	
TRUE	WS_KBD2	48	
TRUE	WS_KBD3	48	
TRUE	WS_KBD4	48	
TRUE	WS_KBD5	48	
TRUE	WS_KBD6	48	
TRUE	WS_KBD7	48	
TRUE	WS_KBD8	48	
TRUE	WS_KBD9	48	
TRUE	WS_KBD10	48	
TRUE	WS_KBD11	48	
TRUE	WS_KBD12	48	
TRUE	WS_KBD13	48	
TRUE	WS_KBD14	48	
TRUE	WS_KBD15_CAP	48	
TRUE	WS_KBD16_NUM	48	
TRUE	WS_KBD17	48	
TRUE	WS_KBD18	48	
TRUE	WS_KBD19	48	
TRUE	WS_KBD20	48	
TRUE	WS_KBD21	48	
TRUE	WS_KBD22	48	
TRUE	WS_KBD23	48	
TRUE	WS_KBD_ONOFF_L	48	
TRUE	WS_LEFT_SHIFT_KBD	48	
TRUE	WS_LEFT_OPTION_KBD	48	
TRUE	WS_CONTROL_KBD	48	
TRUE	KBDLED_ANODE	6 49	
TRUE	GND		2 TPs

Airport/BT/Camera Conn.

FUNC_TEST

TRUE	PCIE_MINI_D2R_P	16 29 77	
TRUE	PCIE_MINI_D2R_N	16 29 77	
TRUE	PCIE_MINI_R2D_P	29 77 82	
TRUE	PCIE_MINI_R2D_N	29 77 82	
TRUE	PCIE_CLK100M_MINI_CONN_P	29 82	
TRUE	PCIE_CLK100M_MINI_CONN_N	29 82	
TRUE	MINI_CLKREQ_Q_L	29	
TRUE	PCIE_WAKE_L	16 29	
TRUE	MINI_RESET_CONN_L	29	
TRUE	PP5V_WLAN	29	
TRUE	PP5V_S3_BTCAMERA_F	29	
TRUE	SMBUS_SMC_A_S3_SDA	6 29 40 43 49 81	
TRUE	SMBUS_SMC_A_S3_SCL	6 29 40 43 49 81	
TRUE	USB_CAMERA_CONN_P	29 82	
TRUE	USB_CAMERA_CONN_N	29 82	
TRUE	CONN_USB2_BT_P	29 82	
TRUE	CONN_USB2_BT_N	29 82	
TRUE	GND		10 TPs

SATA HDD Connector

FUNC_TEST

TRUE	PP5V_S0_HDD_FLT	6 37	4 TPs
TRUE	PP5V_S3_IR_R	37	
TRUE	SATA_HDD_R2D_P	37 77	
TRUE	SATA_HDD_R2D_N	37 77	
TRUE	SATA_HDD_D2R_C_P	37 77	
TRUE	SATA_HDD_D2R_C_N	37 77	
TRUE	IR_RX_OUT	37 39	
TRUE	SYS_LED_ANODE_R	37	
TRUE	GND		6 TPs

KBD Backlight Conn.

FUNC_TEST

TRUE	KBDLED_ANODE	6 49	2 TPs
TRUE	SMC_KDBLED_PRESENT_L	49	
TRUE	GND		

DC Power Connector

FUNC_TEST

TRUE	PP18V5_DCIN_FUSE	59	3 TPs
TRUE	ADAPTER_SENSE	59	
TRUE	GND		3 TPs

Battery Connector

FUNC_TEST

TRUE	PPVBAT_G3H_CONN	59 60	3 TPs
TRUE	SMBUS_SMC_BSA_SCL	6 40 43 59 60 81	
TRUE	SMBUS_SMC_BSA_SDA	6 40 43 59 60 81	
TRUE	SYS_DETECT_L	59	
TRUE	GND_BATT_CHGND	8 59	6 TPs

BIL Connector

FUNC_TEST

TRUE	PP3V42_G3H	42 45 48 59 60 67 42 45 48 59 60 67 21 24 38 40 41 42 43 45	3 TPs
TRUE	SMC_LID_R	59	
TRUE	SMBUS_SMC_BSA_SCL	6 40 43 59 60 81	
TRUE	SMBUS_SMC_BSA_SDA	6 40 43 59 60 81	
TRUE	SMC_BIL_BUTTON_L	40 41 59	
TRUE	GND		3 TPs

Power Nets

FUNC_TEST

TRUE	PPVCORE_S0_CPU	7 10 11 44 61	
TRUE	PPVCORE_S0_MCP	7 21 22 44 64	
TRUE	PP0V75_S0_DDRVTT	7 26 27 63 68	
TRUE	PP1V05_S0	7 9 10 11 12 13 16 17 19 21 22 23 35 61 65 66 67	
TRUE	PP1V5_S0	7 10 11 15 22 37 66 67 68 82	
TRUE	PP1V8_S0	7 17 23 53 66	
TRUE	PP3V3_S0	58 61 66 67 68 69 71 72 82 35 37 41 43 45 46 47 49 53 57	
TRUE	PP1V5_S3	7 26 27 28 63 68	
TRUE	PP3V3_S3	6 7 20 25 29 30 43 48 50 68	
TRUE	PP1V05_S5	6 7 21 22 32 66	
TRUE	PP3V3_S5	7 17 19 21 22 24 28 32 35 36 42 52 62 66 67 68 69 71 82	
TRUE	PP3V42_G3H	6 7 20 21 24 38 40 41 42 43 45 48 59 60 67	
TRUE	PPBUS_G3H	7 35 44 45 59 60 62 63 64 73	
TRUE	PP3V3_ENET	7 17 22 31 32	
TRUE	PP1V05_ENET	7 17 22 31 32	
TRUE	PP5V_S3	7 8 29 37 38 39 41 49 51 53 62 63 68	
TRUE	PP3V3_S5_AVREF_SMC	40 41	
TRUE	PP18V5_S3	6 49	
TRUE	PP3V3_S3_LDO	6 49	
TRUE	PPVOUT_S0_LCDBKLT	6 51 69 72 74	
TRUE	PP4V5_AUDIO_ANALOG	53	
TRUE	SMC_PM_G2_EN	8 40 62 67	
TRUE	PM_SLP_S4_L	20 38 40 41 67	
TRUE	PM_SLP_S3_L	20 32 35 40 67 71	
TRUE	PP1V05_S5	6 7 21 22 32 66	
TRUE	PP5V_SW_ODD	6 37 51	
TRUE	PP5V_S0_HDD_FLT	6 37	
TRUE	BKL_VLDO	72	
TRUE	GND		6 TPs

ICT Test Points

				NO_TEST
53 6	NC_AUD_LO1_N_L	NC_AUD_LO1_N_L		
53 6	NC_AUD_LO1_P_L	NC_AUD_LO1_P_L	MAKE_BASE=TRUE	TRUE 6 53
19 6	NC_USB_10N	NC_USB_10N	MAKE_BASE=TRUE	TRUE 6 19
19 6	NC_USB_10P	NC_USB_10P	MAKE_BASE=TRUE	TRUE 6 19
17 6	NC_ENET_INTR_L	NC_ENET_INTR_L	MAKE_BASE=TRUE	TRUE 6 17
17 6	NC_ENET_PWRDWN_L	NC_ENET_PWRDWN_L	MAKE_BASE=TRUE	TRUE 6 17
48 6	NC_ISSP_SCLK_P1_1	NC_ISSP_SCLK_P1_1	MAKE_BASE=TRUE	TRUE 6 48
48 6	NC_ISSP_SDATA_P1_0	NC_ISSP_SDATA_P1_0	MAKE_BASE=TRUE	TRUE 6 48
6	NC_LCDBKLT_FAIL	NC_LCDBKLT_FAIL	MAKE_BASE=TRUE	TRUE 6
18 6	NC_LPC_DRQ0_L	NC_LPC_DRQ0_L	MAKE_BASE=TRUE	TRUE 6 18
	TP_MEM_A_CKE<3..2>	NC_MEM_A_CKE<3..2>	MAKE_BASE=TRUE	TRUE 15
14 6	NC_MEM_A_CLK2N	NC_MEM_A_CLK2N	MAKE_BASE=TRUE	TRUE 6 14
15 6	NC_MEM_A_CLK3N	NC_MEM_A_CLK3N	MAKE_BASE=TRUE	TRUE 6 15
15 6	NC_MEM_A_CLK3P	NC_MEM_A_CLK3P	MAKE_BASE=TRUE	TRUE 6 15
15 6	NC_MEM_A_CLK4P	NC_MEM_A_CLK4P	MAKE_BASE=TRUE	TRUE 6 15
15 6	NC_MEM_A_CS_L<3>	NC_MEM_A_CS_L<3>	MAKE_BASE=TRUE	TRUE 6 15
	TP_MEM_A_ODT<3..2>	NC_MEM_A_ODT<3..2>	MAKE_BASE=TRUE	TRUE 15
15 6	NC_MEM_B_CKE<2>	NC_MEM_B_CKE<2>	MAKE_BASE=TRUE	TRUE 6 15
15 6	NC_MEM_B_CLK3P	NC_MEM_B_CLK3P	MAKE_BASE=TRUE	TRUE 6 15
15 6	NC_MEM_B_CLK4N	NC_MEM_B_CLK4N	MAKE_BASE=TRUE	TRUE 6 15
15 6	NC_MEM_B_CLK4P	NC_MEM_B_CLK4P	MAKE_BASE=TRUE	TRUE 6 15
15 6	NC_MEM_B_CLK5N	NC_MEM_B_CLK5N	MAKE_BASE=TRUE	TRUE 6 15
15 6	NC_MEM_B_ODT<2>	NC_MEM_B_ODT<2>	MAKE_BASE=TRUE	TRUE 6 15
20 6	NC_MLB_RAM_SIZE	NC_MLB_RAM_SIZE	MAKE_BASE=TRUE	TRUE 6 20
48 6	NC_P7_7	NC_P7_7	MAKE_BASE=TRUE	TRUE 6 48
	TP_PCI_AD<31..8>	NC_PCI_AD<31..8>	MAKE_BASE=TRUE	TRUE 18
	TP_PCI_C_BE_L<3..0>	NC_PCI_C_BE_L<3..0>	MAKE_BASE=TRUE	TRUE 18
18 6	NC_PCI_CLK0	NC_PCI_CLK0		
18 6	NC_PCI_CLK1	NC_PCI_CLK1	MAKE_BASE=TRUE	TRUE 6 18
18 6	NC_PCI_DEVSEL_L	NC_PCI_DEVSEL_L	MAKE_BASE=TRUE	TRUE 6 18
18 6	NC_PCI_FRAME_L	NC_PCI_FRAME_L	MAKE_BASE=TRUE	TRUE 6 18
18 6	NC_PCI_GNT0_L	NC_PCI_GNT0_L	MAKE_BASE=TRUE	TRUE 6 18
18 6	NC_PCI_GNT1_L	NC_PCI_GNT1_L	MAKE_BASE=TRUE	TRUE 6 18
18 6	NC_PCI_INTW_L	NC_PCI_INTW_L	MAKE_BASE=TRUE	TRUE 6 18
18 6	NC_PCI_INTX_L	NC_PCI_INTX_L	MAKE_BASE=TRUE	TRUE 6 18
18 6	NC_PCI_INTZ_L	NC_PCI_INTZ_L	MAKE_BASE=TRUE	TRUE 6 18
18 6	NC_PCI_IRDY_L	NC_PCI_IRDY_L	MAKE_BASE=TRUE	TRUE 6 18
18 6	NC_PCI_PERR_L	NC_PCI_PERR_L	MAKE_BASE=TRUE	TRUE 6 18
18 6	NC_PCI_RESET1_L	NC_PCI_RESET1_L	MAKE_BASE=TRUE	TRUE 6 18
18 6	NC_PCI_SERR_L	NC_PCI_SERR_L	MAKE_BASE=TRUE	TRUE 6 18
18 6	NC_PCI_STOP_L	NC_PCI_STOP_L	MAKE_BASE=TRUE	TRUE 6 18
18 6	NC_PCI_TRDY_L	NC_PCI_TRDY_L	MAKE_BASE=TRUE	TRUE 6 18
16 6	NC_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE	TRUE 6 16
16 6	NC_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE	TRUE 6 16
16 6	NC_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE	TRUE 6 16
16 6	NC_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE	TRUE 6 16
16 6	NC_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE	TRUE 6 16
16 6	NC_PCIE_PE4_D2RN	NC_PCIE_PE4_D2RN	MAKE_BASE=TRUE	TRUE 6 16
16 6	NC_PCIE_PE4_R2D_CN	NC_PCIE_PE4_R2D_CN	MAKE_BASE=TRUE	TRUE 6 16
16 6	NC_PE4_PRSNT_L	NC_PE4_PRSNT_L	MAKE_BASE=TRUE	TRUE 6 16
48 6	NC_PSOC_P1_3	NC_PSOC_P1_3	MAKE_BASE=TRUE	TRUE 6 48
48 6	NC_PSOC_SDA	NC_PSOC_SDA	MAKE_BASE=TRUE	TRUE 6 48
19 6	NC_SATA_C_D2RP	NC_SATA_C_D2RP	MAKE_BASE=TRUE	TRUE 6 19
19 6	NC_SATA_C_R2D_CN	NC_SATA_C_R2D_CN	MAKE_BASE=TRUE	TRUE 6 19
19 6	NC_SATA_C_R2D_CP	NC_SATA_C_R2D_CP	MAKE_BASE=TRUE	TRUE 6 19
19 6	NC_SATA_D_D2RN	NC_SATA_D_D2RN	MAKE_BASE=TRUE	TRUE 6 19
19 6	NC_SATA_D_D2RP	NC_SATA_D_D2RP	MAKE_BASE=TRUE	TRUE 6 19
20 6	NC_SB_A20GATE	NC_SB_A20GATE	MAKE_BASE=TRUE	TRUE 6 20

NO_TEST

TRUE	FSB_A_L<31..3>	9 13 75
TRUE	FSB_ADS_L	9 13 75
TRUE	FSB_ADSTB_L<1..0>	9 13 75
TRUE	FSB_D_L<63..0>	9 13 75
TRUE	FSB_DINV_L<3..0>	9 13 75
TRUE	FSB_DSTB_L_N<3..0>	9 13 75
TRUE	FSB_DSTB_L_P<3..0>	9 13 75
TRUE	FSB_HIT_L	9 13 75
TRUE	FSB_HITM_L	9 13 75
TRUE	FSB_LOCK_L	9 13 75
TRUE	FSB_REQ_L<4..0>	13 75 9
TRUE	MCPCORES0_OCSET	
TRUE	USB_BT_N	19 29 78
TRUE	USB_BT_P	19 29 78
TRUE	USB_CAMERA_N	19 29 78
TRUE	USB_CAMERA_P	19 29 78
TRUE	SATA_ODD_D2R_UF_N	37 82
TRUE	SATA_ODD_D2R_UF_P	37 82
TRUE	DP_ML_C_P<3..0>	71 82

Note.
NO_TEST properties are also on page9,26,43,50

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Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

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"G3Hot" (Always-Present) Rails

PPBUS_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE

PPBUS_CPU_IMVP_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE

PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE

DCIN Rail

PPDCIN_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

"FW" (FireWire) Rail

PPVP_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.0V
MAKE_BASE=TRUE

5V Rails

PP5V_S3
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE

MCP79 PCIe/SATA Rails

PP1V05_S0
PP1V05_S0_MCP_PEX_AVDD
MAKE_BASE=TRUE
PP1V05_S0
PP1V05_S0_MCP_SATA_AVDD
MAKE_BASE=TRUE

3.3V Rails

PP3V3_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S3
MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_ENET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_FW
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

1.8V Rail

PP1V8_S0
500 mA max supply
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
190 mA

1.5V S3 Rail

PP1V5_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

1.5V S0 Rail

PP1V5_S0
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
130 mA
4771 mA

DDR3 Reference Plane

GND
GND
K19i uses GND reference for ALL DDR3 signals.

1.05V Rails

PP1V05_S5
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
105 mA/241 mA
139 mA/ 0 mA

PP1V05_ENET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V05_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
4500 mA
1182 mA
1034 mA
6600 MA
241 mA max load

PP1V05_S0_MCP_PLL_UF
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V05_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

Chipset "VCore" Rails

PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE

PPVCORE_S0_MCP
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

0.75V Rails

PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

PP0V75_S0_DDRVTT
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

Power Aliases

SYNC_MASTER=N/A SYNC_DATE=N/A

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Board Mounting Holes

(Not to scale)

ZT0965 HOLE-VIA-P5RP25
ZT0960 3R2P5
ZT0950 TH SL-3.1X2.7-6CIR-NSP
ZT0942 3R2P5
ZT0940 3R2P5
ZT0990 3R2P5 (ORIGIN)
ZT0915 3R2P5
ZT0945 HOLE-VIA-P5RP25

NOTE: VIAs represent non-plated holes with ground rings.
Place VIAs in corresponding hole's ground ring.

Left Speaker Standoffs

ZT0934 STDOFF-4.0OD3.0H-TH (UPPER)
ZT0935 STDOFF-4.0OD3.0H-TH (LOWER)

I/O Row Pogos

SH0914 1.4DIA-SHORT-EMI-MLB-M97-M98 SM (Ethernet)
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98 SM (FW800)
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98 SM (Mini-DP)
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98 SM (Upper USB)
SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98 SM (Lower USB)
SH0915 1.4DIA-SHORT-EMI-MLB-M97-M98 SM (SD Card)
SH0916 1.4DIA-SHORT-EMI-MLB-M97-M98 SM (Audio)

GND_CHASSIS_AUDIO_JACK 57

Digital Ground

GND_BATT_CHGND 6 59
GND
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=0V

CPU Thermal Module Holes

ZT0985 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0986 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0981 STDOFF-4.5OD.98H-1.1-3.48-TH

MCP Thermal Module Holes

ZT0930 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0982 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0984 STDOFF-4.5OD.98H-1.1-3.48-TH

Fan Screw Hole

ZT0988 STDOFF-4.5OD.98H-1.1-3.48-TH

CPU Pogo

SH0903 2.0DIA-TALL-EMI-MLB-M97-M98 SM

SO-DIMM Pogos

SH0900 2.0DIA-TALL-EMI-MLB-M97-M98 SM (LEFT)
SH0902 2.0DIA-TALL-EMI-MLB-M97-M98 SM (RIGHT)

Other Board Pogos

SH0905 2.0DIA-TALL-EMI-MLB-M97-M98 SM (Near BIL Connector)
SH0906 2.0DIA-TALL-EMI-MLB-M97-M98 SM (Near IPD Connector)

Bosses

ZT0951 4.0OD1.85H-M1.6X0.35 (Keyboard Protector)
ZT0952 4.0OD1.85H-M1.6X0.35 (IPD Protector)

CPU Signals

TP_IMVP6_CLKEN_L — TP_IMVP6_CLKEN_L MAKE_BASE=TRUE
CPU_VID<0..6> — IMVP6_VID<0..6> MAKE_BASE=TRUE
CPU_BSEL<0..2> — =MCP_BSEL<0..2> MAKE_BASE=TRUE
TP_CPU_PECI_MCP — TP_CPU_PECI_MCP MAKE_BASE=TRUE

PEG Signals

NC_PEG_CLK100MP — NC_PEG_CLK100MP MAKE_BASE=TRUE NO_TEST=TRUE
NC_PEG_CLK100MN — NC_PEG_CLK100MN MAKE_BASE=TRUE NO_TEST=TRUE
=PEG_R2D_C_P<0..15> — NC_PEG_R2DCP<0..15> MAKE_BASE=TRUE NO_TEST=TRUE
=PEG_R2D_C_N<0..15> — NC_PEG_R2DCN<0..15> MAKE_BASE=TRUE NO_TEST=TRUE
NC_PEG_D2RP<0..15> — =PEG_D2R_P<0..15> MAKE_BASE=TRUE NO_TEST=TRUE
NC_PEG_D2RN<0..15> — =PEG_D2R_N<0..15> MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEG_PRSNT_L — TP_PEG_PRSNT_L MAKE_BASE=TRUE (Internal pull-up)

PCIe Signals

NC_PCIE_CLK100M_EXCARDP — NC_PCIE_CLK100M_EXCARDP MAKE_BASE=TRUE NO_TEST=TRUE
NC_PCIE_CLK100M_EXCARDN — NC_PCIE_CLK100M_EXCARDN MAKE_BASE=TRUE NO_TEST=TRUE
TP_EXCARD_CLKREQ_L — TP_EXCARD_CLKREQ_L MAKE_BASE=TRUE (Internal pull-up)
NC_PCIE_EXCARD_R2DCP — NC_PCIE_EXCARD_R2DCP MAKE_BASE=TRUE NO_TEST=TRUE
NC_PCIE_EXCARD_R2DCN — NC_PCIE_EXCARD_R2DCN MAKE_BASE=TRUE NO_TEST=TRUE
NC_PCIE_EXCARD_D2RP — NC_PCIE_EXCARD_D2RP MAKE_BASE=TRUE NO_TEST=TRUE
NC_PCIE_EXCARD_D2RN — NC_PCIE_EXCARD_D2RN MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCIE_EXCARD_PRSNT_L — TP_PCIE_EXCARD_PRSNT_L MAKE_BASE=TRUE (Internal pull-up)
PCIE_FW_PRSNT_L
NOSTUFF R0925 0 5% 1/16W ME-LF 402

LVDS Signals

LVDS_CONN_A_CLK_P — LVDS_CONN_A_CLK_P MAKE_BASE=TRUE
LVDS_CONN_A_CLK_N — LVDS_CONN_A_CLK_N MAKE_BASE=TRUE
LVDS_IG_A_DATA_P<0..2> — LVDS_CONN_A_DATA_P<0..2> MAKE_BASE=TRUE
LVDS_IG_A_DATA_N<0..2> — LVDS_CONN_A_DATA_N<0..2> MAKE_BASE=TRUE
NC_LVDS_IG_A_DATAP<3> — NC_LVDS_IG_A_DATAP<3> MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_IG_A_DATAN<3> — NC_LVDS_IG_A_DATAN<3> MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_CONN_B_CLK_P — LVDS_CONN_B_CLK_P MAKE_BASE=TRUE
LVDS_CONN_B_CLK_N — LVDS_CONN_B_CLK_N MAKE_BASE=TRUE
LVDS_IG_B_DATA_P<0..2> — LVDS_CONN_B_DATA_P<0..2> MAKE_BASE=TRUE
LVDS_IG_B_DATA_N<0..2> — LVDS_CONN_B_DATA_N<0..2> MAKE_BASE=TRUE
NC_LVDS_IG_B_DATAP<3> — NC_LVDS_IG_B_DATAP<3> MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_IG_B_DATAN<3> — NC_LVDS_IG_B_DATAN<3> MAKE_BASE=TRUE NO_TEST=TRUE
LVDS_BKL_ON — LVDS_BKL_ON MAKE_BASE=TRUE
LCD_BKLT_PWM — LCD_BKLT_PWM MAKE_BASE=TRUE
LCD_PWR_EN — LCD_PWR_EN MAKE_BASE=TRUE
LVDS_DDC_CLK — LVDS_DDC_CLK MAKE_BASE=TRUE
LVDS_DDC_DATA — LVDS_DDC_DATA MAKE_BASE=TRUE

DisplayPort Signals

(Aliases on page70.csa)

FireWire Signals

FW643_WAKE_L — FW643_WAKE_L MAKE_BASE=TRUE
FW_PLUG_DET_L — FW_PLUG_DET_L MAKE_BASE=TRUE

Memory Signals

MEM_VTT_EN — MEM_VTT_EN MAKE_BASE=TRUE
NC_MEM_A_A<15> — NC_MEM_A_A<15> MAKE_BASE=TRUE NO_TEST=TRUE
NC_MEM_B_A<15> — NC_MEM_B_A<15> MAKE_BASE=TRUE NO_TEST=TRUE

USB Signals

NC_USB_EXTCP — NC_USB_EXTCP MAKE_BASE=TRUE NO_TEST=TRUE
NC_USB_EXTCN — NC_USB_EXTCN MAKE_BASE=TRUE NO_TEST=TRUE
NC_USB_EXTDP — NC_USB_EXTDP MAKE_BASE=TRUE NO_TEST=TRUE
NC_USB_EXTDN — NC_USB_EXTDN MAKE_BASE=TRUE NO_TEST=TRUE
NC_USB_MINIP — NC_USB_MINIP MAKE_BASE=TRUE NO_TEST=TRUE
NC_USB_MININ — NC_USB_MININ MAKE_BASE=TRUE NO_TEST=TRUE
NC_USB_EXCARDP — NC_USB_EXCARDP MAKE_BASE=TRUE NO_TEST=TRUE
NC_USB_EXCARDN — NC_USB_EXCARDN MAKE_BASE=TRUE NO_TEST=TRUE

Audio Signals

AUD_IPHS_SWITCH_EN
R0902 10K 5% 1/16W ME-LF 402

XW0901 SM
PP5V_S3 — PP5V_S3_AUDIO_AMP
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

Ethernet Signals

PM_SLP_RMGT_L — PM_SLP_RMGT_L MAKE_BASE=TRUE
NC_RTL8211_REGOUT — NC_RTL8211_REGOUT MAKE_BASE=TRUE NO_TEST=TRUE
RTL8211_VDDREG — RTL8211_VDDREG MAKE_BASE=TRUE
GND
MCP_MII_PD
R0930 47K 5% 1/16W ME-LF 402
RTL8211_CLK125 — RTL8211_CLK125 MAKE_BASE=TRUE
R0931 22 5% 1/16W ME-LF 402

Power Signals

SMC_PM_G2_EN — SMC_PM_G2_EN MAKE_BASE=TRUE

GMUX Signals

TP_GMUX_JTAG_TCK_L — TP_GMUX_JTAG_TCK_L MAKE_BASE=TRUE
TP_GMUX_JTAG_TDI — TP_GMUX_JTAG_TDI MAKE_BASE=TRUE
TP_GMUX_JTAG_TMS — TP_GMUX_JTAG_TMS MAKE_BASE=TRUE
TP_GMUX_JTAG_TDO — TP_GMUX_JTAG_TDO MAKE_BASE=TRUE
MCP_HPLUG_DET2 — MCP_HPLUG_DET2 MAKE_BASE=TRUE
R0920 20K 5% 1/16W ME-LF 402

Signal Aliases

SYNC_MASTER=WFERRY_K19I SYNC_DATE=01/13/2009

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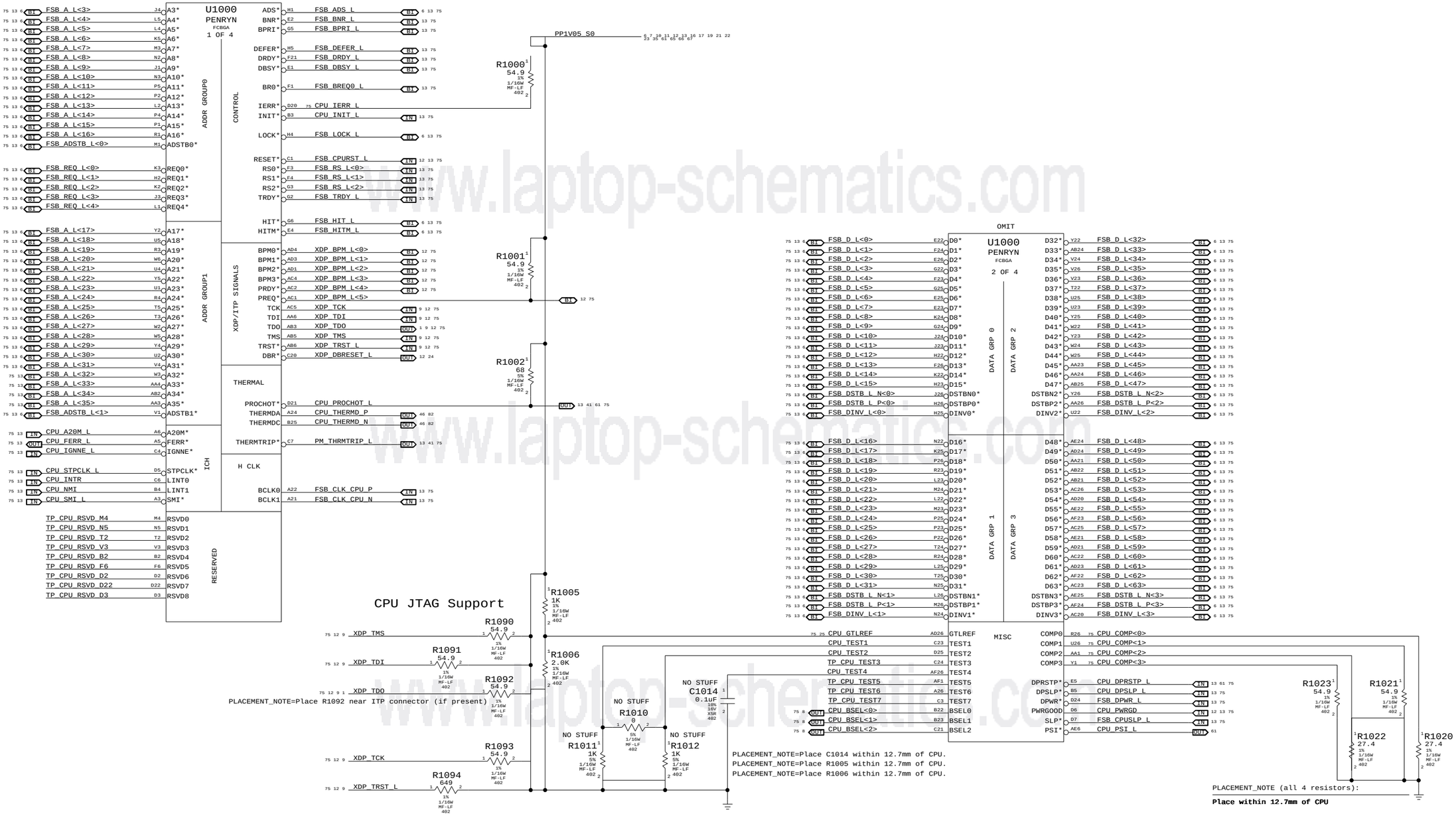
SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE: NONE	SHT 8 OF 83	



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SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

CPU FSB

SYNC_MASTER=K24_MLB SYNC_DATE=02/05/2009

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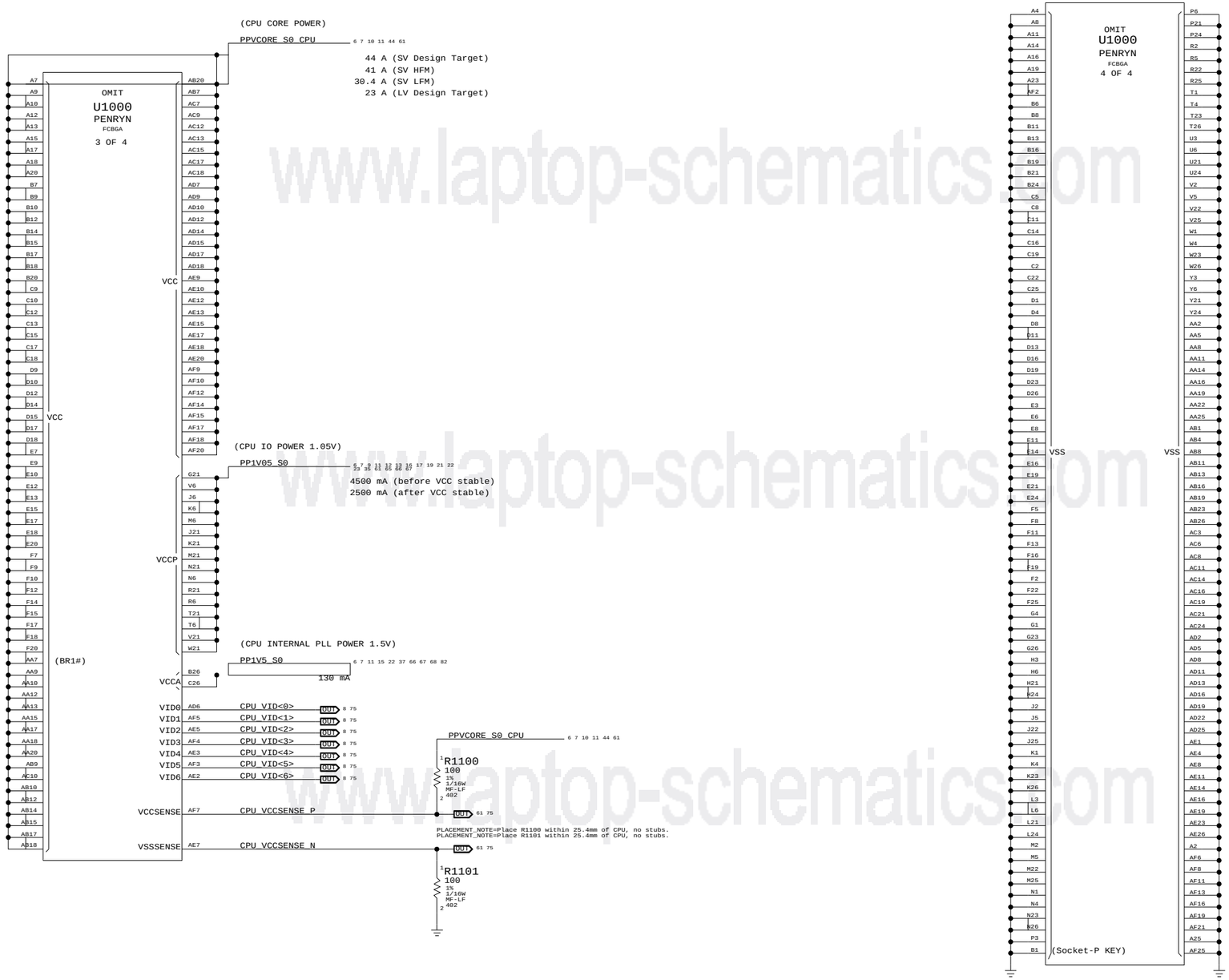

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SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

CPU Power & Ground

SYNC_MASTER=K24_MLB SYNC_DATE=02/05/2009

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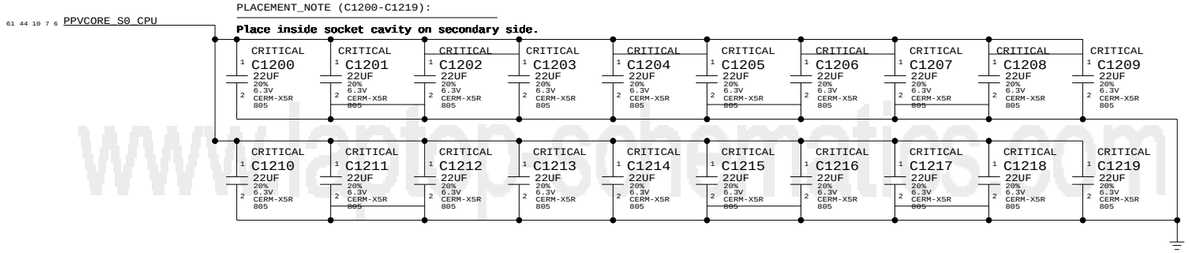
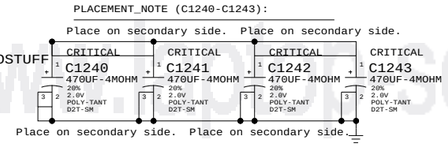
D	051-7903	A

SCALE	SHT	OF
NONE	10	83

CPU VCore HF and Bulk Decoupling

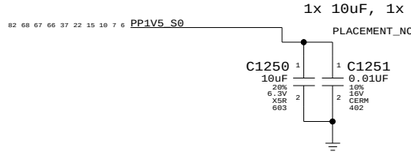
4X 330UF. 20X 22UF 0805





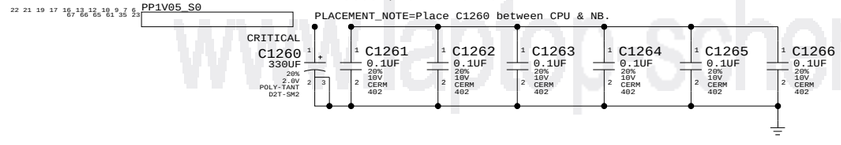
VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402



SYNC FROM T18
REMOVE NO STUFF CAPS C1220 TO C1231
REMOVE C1244 & C1245
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

CPU Decoupling

SYNC_MASTER=K24_MLB SYNC_DATE=02/05/2009

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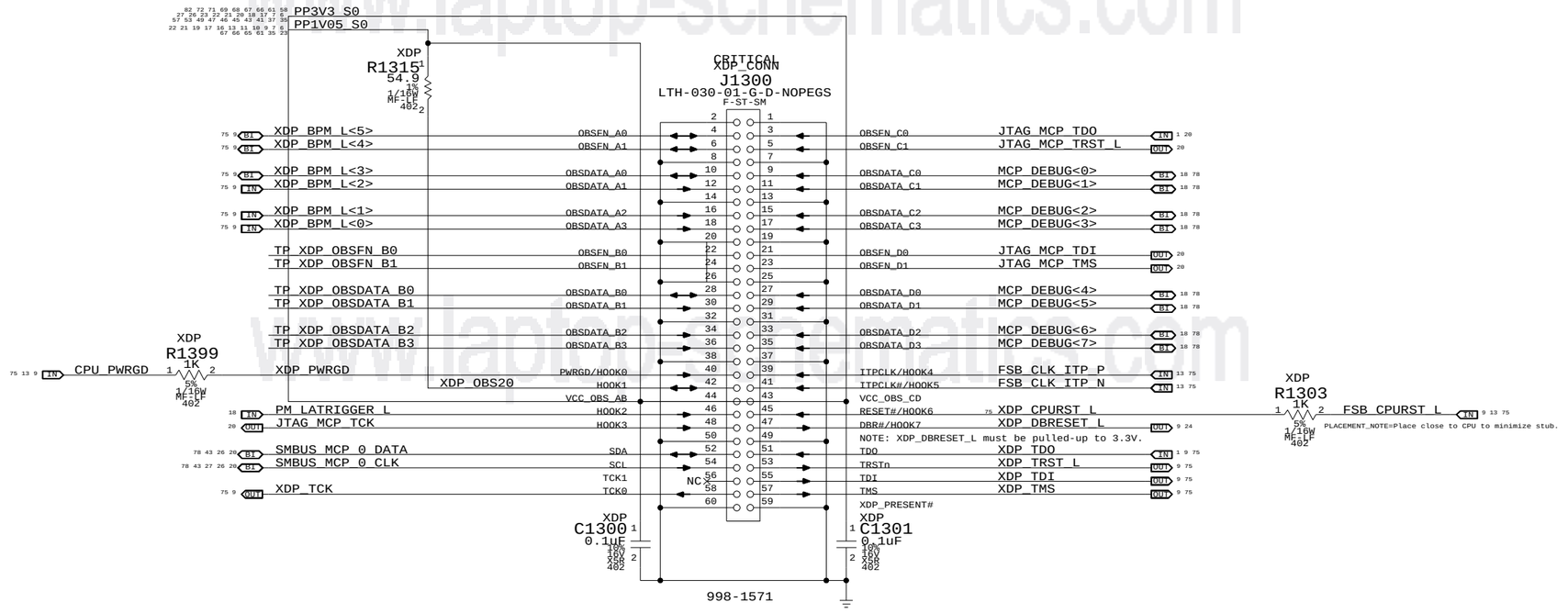
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

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eXtended Debug Port(MiniXDP)

SYNC_MASTER=K19_MLB SYNC_DATE=02/05/2009

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OMIT

U1400
MCP79-TOPO-B
BGA
(1 OF 11)

FSB

FSB_DSTB_L_P<0>	T40	CPU_DSTBP0#	
FSB_DSTB_L_N<0>	U40	CPU_DSTBN0#	
FSB_DINV_L<0>	V41	CPU_DBI0#	
FSB_DSTB_L_P<1>	W39	CPU_DSTBP1#	
FSB_DSTB_L_N<1>	W37	CPU_DSTBN1#	
FSB_DINV_L<1>	V35	CPU_DBI1#	
FSB_DSTB_L_P<2>	N37	CPU_DSTBP2#	
FSB_DSTB_L_N<2>	L36	CPU_DSTBN2#	
FSB_DINV_L<2>	N35	CPU_DBI2#	
FSB_DSTB_L_P<3>	M39	CPU_DSTBP3#	
FSB_DSTB_L_N<3>	M41	CPU_DSTBN3#	
FSB_DINV_L<3>	J41	CPU_DBI3#	
FSB_A_L<3>	AC34	CPU_A3#	
FSB_A_L<4>	AE38	CPU_A4#	
FSB_A_L<5>	AE34	CPU_A5#	
FSB_A_L<6>	AC37	CPU_A6#	
FSB_A_L<7>	AE37	CPU_A7#	
FSB_A_L<8>	AE35	CPU_A8#	
FSB_A_L<9>	AB35	CPU_A9#	
FSB_A_L<10>	AF35	CPU_A10#	
FSB_A_L<11>	AG35	CPU_A11#	
FSB_A_L<12>	AG39	CPU_A12#	
FSB_A_L<13>	AE33	CPU_A13#	
FSB_A_L<14>	AG37	CPU_A14#	
FSB_A_L<15>	AG38	CPU_A15#	
FSB_A_L<16>	AG34	CPU_A16#	
FSB_A_L<17>	AN38	CPU_A17#	
FSB_A_L<18>	AL39	CPU_A18#	
FSB_A_L<19>	AG33	CPU_A19#	
FSB_A_L<20>	AL33	CPU_A20#	
FSB_A_L<21>	AJ33	CPU_A21#	
FSB_A_L<22>	AN36	CPU_A22#	
FSB_A_L<23>	AJ35	CPU_A23#	
FSB_A_L<24>	AJ37	CPU_A24#	
FSB_A_L<25>	AJ36	CPU_A25#	
FSB_A_L<26>	AJ38	CPU_A26#	
FSB_A_L<27>	AL37	CPU_A27#	
FSB_A_L<28>	AL34	CPU_A28#	
FSB_A_L<29>	AN37	CPU_A29#	
FSB_A_L<30>	AJ34	CPU_A30#	
FSB_A_L<31>	AL38	CPU_A31#	
FSB_A_L<32>	AL35	CPU_A32#	
FSB_A_L<33>	AN34	CPU_A33#	
FSB_A_L<34>	AR39	CPU_A34#	
FSB_A_L<35>	AN35	CPU_A35#	
FSB_ADSTB_L<0>	AE36	CPU_ADSTB0#	
FSB_ADSTB_L<1>	AK35	CPU_ADSTB1#	
FSB_REQ_L<0>	AC38	CPU_REQ0#	
FSB_REQ_L<1>	AA33	CPU_REQ1#	
FSB_REQ_L<2>	AC39	CPU_REQ2#	
FSB_REQ_L<3>	AC33	CPU_REQ3#	
FSB_REQ_L<4>	AC35	CPU_REQ4#	
FSB_ADS_L	AD42	CPU_ADS#	
FSB_BNR_L	AD43	CPU_BNR#	
FSB_BREQ0_L	AE40	CPU_BR0#	
FSB_BREQ1_L	AL32	CPU_BR1#	
FSB_DBSY_L	AD39	CPU_DBSY#	
FSB_DRDY_L	AD41	CPU_DRDY#	
FSB_HIT_L	AB42	CPU_HIT#	
FSB_HITM_L	AD40	CPU_HITM#	
FSB_LOCK_L	AC43	CPU_LOCK#	
FSB_TRDY_L	AE41	CPU_TRDY#	
TP_CPU_PECI_MCP	E41	CPU_PECI	
CPU_PROCHOT_L	AJ41	CPU_PROCHOT#	
	AG43	CPU_THERMTRIP#	
	AH40	CPU_FERR#	
(MCP_BSEL<2>)	F42	CPU_BSEL2	
(MCP_BSEL<1>)	D42	CPU_BSEL1	
(MCP_BSEL<0>)	F41	CPU_BSEL0	
FSB_RS_L<0>	AC41	CPU_RS0#	
FSB_RS_L<1>	AB41	CPU_RS1#	
FSB_RS_L<2>	AC42	CPU_RS2#	
PP1V05_S0_MCP_PLL_FSB 270 mA (A01)	AG27	+V_DLL_DLCELL_AVDD	206 mA
	AH27	+V_PLL_MCLK	20 mA
	AG28	+V_PLL_FSB	29 mA
	AH28	+V_PLL_CPU	15 mA
MCP_BCLK_VML_COMP_VDD	AM39	BCLK_VML_COMP_VDD	
MCP_BCLK_VML_COMP_GND	AM40	BCLK_VML_COMP_GND	
MCP_CPU_COMP_VCC	AM43	CPU_COMP_VCC	
MCP_CPU_COMP_GND	AM42	CPU_COMP_GND	

CPU_D0#	Y43	FSB_D_L<0>	
CPU_D1#	W42	FSB_D_L<1>	
CPU_D2#	Y40	FSB_D_L<2>	
CPU_D3#	W41	FSB_D_L<3>	
CPU_D4#	Y39	FSB_D_L<4>	
CPU_D5#	V42	FSB_D_L<5>	
CPU_D6#	Y41	FSB_D_L<6>	
CPU_D7#	Y42	FSB_D_L<7>	
CPU_D8#	P42	FSB_D_L<8>	
CPU_D9#	U41	FSB_D_L<9>	
CPU_D10#	R42	FSB_D_L<10>	
CPU_D11#	T39	FSB_D_L<11>	
CPU_D12#	T42	FSB_D_L<12>	
CPU_D13#	T41	FSB_D_L<13>	
CPU_D14#	R41	FSB_D_L<14>	
CPU_D15#	T43	FSB_D_L<15>	
CPU_D16#	W35	FSB_D_L<16>	
CPU_D17#	AA37	FSB_D_L<17>	
CPU_D18#	W33	FSB_D_L<18>	
CPU_D19#	W34	FSB_D_L<19>	
CPU_D20#	AA36	FSB_D_L<20>	
CPU_D21#	AA34	FSB_D_L<21>	
CPU_D22#	AA38	FSB_D_L<22>	
CPU_D23#	AA35	FSB_D_L<23>	
CPU_D24#	U38	FSB_D_L<24>	
CPU_D25#	U36	FSB_D_L<25>	
CPU_D26#	U35	FSB_D_L<26>	
CPU_D27#	U33	FSB_D_L<27>	
CPU_D28#	U34	FSB_D_L<28>	
CPU_D29#	W38	FSB_D_L<29>	
CPU_D30#	R33	FSB_D_L<30>	
CPU_D31#	U37	FSB_D_L<31>	
CPU_D32#	N34	FSB_D_L<32>	
CPU_D33#	N33	FSB_D_L<33>	
CPU_D34#	R34	FSB_D_L<34>	
CPU_D35#	R35	FSB_D_L<35>	
CPU_D36#	P35	FSB_D_L<36>	
CPU_D37#	R39	FSB_D_L<37>	
CPU_D38#	R37	FSB_D_L<38>	
CPU_D39#	R38	FSB_D_L<39>	
CPU_D40#	L37	FSB_D_L<40>	
CPU_D41#	L39	FSB_D_L<41>	
CPU_D42#	L38	FSB_D_L<42>	
CPU_D43#	N36	FSB_D_L<43>	
CPU_D44#	N38	FSB_D_L<44>	
CPU_D45#	J39	FSB_D_L<45>	
CPU_D46#	J38	FSB_D_L<46>	
CPU_D47#	J37	FSB_D_L<47>	
CPU_D48#	L42	FSB_D_L<48>	
CPU_D49#	M42	FSB_D_L<49>	
CPU_D50#	P41	FSB_D_L<50>	
CPU_D51#	N41	FSB_D_L<51>	
CPU_D52#	N40	FSB_D_L<52>	
CPU_D53#	M40	FSB_D_L<53>	
CPU_D54#	H40	FSB_D_L<54>	
CPU_D55#	K42	FSB_D_L<55>	
CPU_D56#	H41	FSB_D_L<56>	
CPU_D57#	L41	FSB_D_L<57>	
CPU_D58#	H43	FSB_D_L<58>	
CPU_D59#	H42	FSB_D_L<59>	
CPU_D60#	K41	FSB_D_L<60>	
CPU_D61#	J40	FSB_D_L<61>	
CPU_D62#	H39	FSB_D_L<62>	
CPU_D63#	M43	FSB_D_L<63>	
CPU_BPRI#	AA41	FSB_BPRI_L	
CPU_DEFER#	AA40	FSB_DEFER_L	
BCLK_OUT_CPU_P	G42	FSB_CLK_CPU_P	
BCLK_OUT_CPU_N	G41	FSB_CLK_CPU_N	
BCLK_OUT_ITP_P	AL43	FSB_CLK_ITP_P	
BCLK_OUT_ITP_N	AL42	FSB_CLK_ITP_N	
BCLK_OUT_NB_P	AL41	FSB_CLK_MCP_P	
BCLK_OUT_NB_N	AK42	FSB_CLK_MCP_N	
BCLK_IN_N	AK41		
BCLK_IN_P	AJ40		
CPU_A20M#	AF41	CPU_A20M_L	
CPU_IGNNE#	AH39	CPU_IGNNE_L	
CPU_INIT#	AH42	CPU_INIT_L	
CPU_INTR	AF42	CPU_INTR	
CPU_NMI	AG41	CPU_NMI	
CPU_SMI#	AH41	CPU_SMI_L	
CPU_PWRGD	AH43	CPU_PWRGD	
CPU_RESET#	H38	FSB_CPURST_L	
CPU_SLP#	AM33	FSB_CPUSLP_L	
CPU_DPSLP#	AN33	CPU_DPSLP_L	
CPU_DPWR#	AM32	FSB_DPWR_L	
CPU_STPCLK#	AG42	CPU_STPCLK_L	
CPU_DPRSTP#	AN32	CPU_DPRSTP_L	

PP1V05_S0
R1410 54.9 1% 1/16W MF-LF 402
R1415 62 5% 1/16W MF-LF 402
R1416 62 5% 1/16W MF-LF 402

PM_THRMTRIP_L
CPU_FERR_L

NO STUFF
R1420 1K 5% 1/16W MF-LF 402
R1421 1K 5% 1/16W MF-LF 402
R1422 1K 5% 1/16W MF-LF 402

=MCP_BSEL<2>
=MCP_BSEL<1>
=MCP_BSEL<0>

R1430 49.9 1% 1/16W MF-LF 402
R1435 49.9 1% 1/16W MF-LF 402
R1431 49.9 1% 1/16W MF-LF 402
R1436 49.9 1% 1/16W MF-LF 402

Loop-back clock for delay matching.

PP1V05_S0
NO STUFF
R1440 150 5% 1/16W MF-LF 402

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP CPU Interface

SYNC_MASTER=T18_MLB SYNC_DATE=02/05/2009

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MCP79-TOPO-B
BGA
(2 OF 11)

MEMORY PARTITION 0

MEM_A_DQ<63>	AL8	MDQ0_63	MDQS0_7_P	AL10	MEM_A_DQS_P<7>
MEM_A_DQ<62>	AL9	MDQ0_62	MDQS0_7_N	AL11	MEM_A_DQS_N<7>
MEM_A_DQ<61>	AP9	MDQ0_61	MDQS0_6_P	AR8	MEM_A_DQS_P<6>
MEM_A_DQ<60>	AN9	MDQ0_60	MDQS0_6_N	AR9	MEM_A_DQS_N<6>
MEM_A_DQ<59>	AL6	MDQ0_59	MDQS0_5_P	AW7	MEM_A_DQS_P<5>
MEM_A_DQ<58>	AL7	MDQ0_58	MDQS0_5_N	AW8	MEM_A_DQS_N<5>
MEM_A_DQ<57>	AN6	MDQ0_57	MDQS0_4_P	AP13	MEM_A_DQS_P<4>
MEM_A_DQ<56>	AN7	MDQ0_56	MDQS0_4_N	AR13	MEM_A_DQS_N<4>
MEM_A_DQ<55>	AR6	MDQ0_55	MDQS0_3_P	AV25	MEM_A_DQS_P<3>
MEM_A_DQ<54>	AR7	MDQ0_54	MDQS0_3_N	AW25	MEM_A_DQS_N<3>
MEM_A_DQ<53>	AV6	MDQ0_53	MDQS0_2_P	AU30	MEM_A_DQS_P<2>
MEM_A_DQ<52>	AW5	MDQ0_52	MDQS0_2_N	AU29	MEM_A_DQS_N<2>
MEM_A_DQ<51>	AN10	MDQ0_51	MDQS0_1_P	AT35	MEM_A_DQS_P<1>
MEM_A_DQ<50>	AR5	MDQ0_50	MDQS0_1_N	AU35	MEM_A_DQS_N<1>
MEM_A_DQ<49>	AU6	MDQ0_49	MDQS0_0_P	AU39	MEM_A_DQS_P<0>
MEM_A_DQ<48>	AV5	MDQ0_48	MDQS0_0_N	AT39	MEM_A_DQS_N<0>
MEM_A_DQ<47>	AU7	MDQ0_47			
MEM_A_DQ<46>	AU8	MDQ0_46			
MEM_A_DQ<45>	AW9	MDQ0_45			
MEM_A_DQ<44>	AP11	MDQ0_44			
MEM_A_DQ<43>	AW6	MDQ0_43			
MEM_A_DQ<42>	AY5	MDQ0_42	MRAS0#	AV17	MEM_A_RAS_L
MEM_A_DQ<41>	AU9	MDQ0_41	MCAS0#	AP17	MEM_A_CAS_L
MEM_A_DQ<40>	AV9	MDQ0_40	MWE0#	AR17	MEM_A_WE_L
MEM_A_DQ<39>	AU11	MDQ0_39			
MEM_A_DQ<38>	AV11	MDQ0_38			
MEM_A_DQ<37>	AV13	MDQ0_37			
MEM_A_DQ<36>	AW13	MDQ0_36			
MEM_A_DQ<35>	AR11	MDQ0_35			
MEM_A_DQ<34>	AT11	MDQ0_34	MBA0_2	AP23	MEM_A_BA<2>
MEM_A_DQ<33>	AR14	MDQ0_33	MBA0_1	AP19	MEM_A_BA<1>
MEM_A_DQ<32>	AU13	MDQ0_32	MBA0_0	AW17	MEM_A_BA<0>
MEM_A_DQ<31>	AR26	MDQ0_31			
MEM_A_DQ<30>	AU25	MDQ0_30			
MEM_A_DQ<29>	AT27	MDQ0_29			
MEM_A_DQ<28>	AU27	MDQ0_28			
MEM_A_DQ<27>	AP25	MDQ0_27			
MEM_A_DQ<26>	AR25	MDQ0_26	MA0_14	AR23	MEM_A_A<14>
MEM_A_DQ<25>	AP27	MDQ0_25	MA0_13	AU15	MEM_A_A<13>
MEM_A_DQ<24>	AR27	MDQ0_24	MA0_12	AN23	MEM_A_A<12>
MEM_A_DQ<23>	AP29	MDQ0_23	MA0_11	AW21	MEM_A_A<11>
MEM_A_DQ<22>	AR29	MDQ0_22	MA0_10	AN19	MEM_A_A<10>
MEM_A_DQ<21>	AP31	MDQ0_21	MA0_9	AV21	MEM_A_A<9>
MEM_A_DQ<20>	AR31	MDQ0_20	MA0_8	AR22	MEM_A_A<8>
MEM_A_DQ<19>	AV27	MDQ0_19	MA0_7	AU21	MEM_A_A<7>
MEM_A_DQ<18>	AN29	MDQ0_18	MA0_6	AP21	MEM_A_A<6>
MEM_A_DQ<17>	AV29	MDQ0_17	MA0_5	AR21	MEM_A_A<5>
MEM_A_DQ<16>	AN31	MDQ0_16	MA0_4	AN21	MEM_A_A<4>
MEM_A_DQ<15>	AU31	MDQ0_15	MA0_3	AV19	MEM_A_A<3>
MEM_A_DQ<14>	AR33	MDQ0_14	MA0_2	AU19	MEM_A_A<2>
MEM_A_DQ<13>	AV37	MDQ0_13	MA0_1	AT19	MEM_A_A<1>
MEM_A_DQ<12>	AW37	MDQ0_12	MA0_0	AR19	MEM_A_A<0>
MEM_A_DQ<11>	AT31	MDQ0_11			
MEM_A_DQ<10>	AV31	MDQ0_10			
MEM_A_DQ<9>	AT37	MDQ0_9			
MEM_A_DQ<8>	AU37	MDQ0_8			
MEM_A_DQ<7>	AW39	MDQ0_7			
MEM_A_DQ<6>	AV39	MDQ0_6			
MEM_A_DQ<5>	AR37	MDQ0_5			
MEM_A_DQ<4>	AR38	MDQ0_4			
MEM_A_DQ<3>	AV38	MDQ0_3			
MEM_A_DQ<2>	AW38	MDQ0_2			
MEM_A_DQ<1>	AR35	MDQ0_1			
MEM_A_DQ<0>	AP35	MDQ0_0			
MEM_A_DM<7>	AN5	MDQM0_7			
MEM_A_DM<6>	AU5	MDQM0_6			
MEM_A_DM<5>	AR10	MDQM0_5			
MEM_A_DM<4>	AN13	MDQM0_4			
MEM_A_DM<3>	AN27	MDQM0_3			
MEM_A_DM<2>	AW29	MDQM0_2			
MEM_A_DM<1>	AV35	MDQM0_1			
MEM_A_DM<0>	AR34	MDQM0_0			

MEMORY CONTROL 0A

MCLK0A_2_P	AW33	TP_MEM_A_CLK2P
MCLK0A_2_N	AV33	NC_MEM_A_CLK2N
MCLK0A_1_P	BA24	MEM_A_CLK_P<1>
MCLK0A_1_N	AY24	MEM_A_CLK_N<1>
MCLK0A_0_P	BB20	MEM_A_CLK_P<0>
MCLK0A_0_N	BC20	MEM_A_CLK_N<0>
MCS0A_1#	AT15	MEM_A_CS_L<1>
MCS0A_0#	AR18	MEM_A_CS_L<0>
MODT0A_1	AP15	MEM_A_ODT<1>
MODT0A_0	AV15	MEM_A_ODT<0>
MCKE0A_1	AU23	MEM_A_CKE<1>
MCKE0A_0	AT23	MEM_A_CKE<0>

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MEMORY PARTITION 1

MEM_B_DQ<63>	AT4	MDQ1_63	MDQS1_7_P	AT2	MEM_B_DQS_P<7>
MEM_B_DQ<62>	AT3	MDQ1_62	MDQS1_7_N	AT1	MEM_B_DQS_N<7>
MEM_B_DQ<61>	AV2	MDQ1_61	MDQS1_6_P	AY2	MEM_B_DQS_P<6>
MEM_B_DQ<60>	AV3	MDQ1_60	MDQS1_6_N	AY1	MEM_B_DQS_N<6>
MEM_B_DQ<59>	AR4	MDQ1_59	MDQS1_5_P	BB6	MEM_B_DQS_P<5>
MEM_B_DQ<58>	AR3	MDQ1_58	MDQS1_5_N	BA6	MEM_B_DQS_N<5>
MEM_B_DQ<57>	AU2	MDQ1_57	MDQS1_4_P	BA10	MEM_B_DQS_P<4>
MEM_B_DQ<56>	AU3	MDQ1_56	MDQS1_4_N	AY11	MEM_B_DQS_N<4>
MEM_B_DQ<55>	AY4	MDQ1_55	MDQS1_3_P	BB33	MEM_B_DQS_P<3>
MEM_B_DQ<54>	AY3	MDQ1_54	MDQS1_3_N	BA33	MEM_B_DQS_N<3>
MEM_B_DQ<53>	BB3	MDQ1_53	MDQS1_2_P	BB37	MEM_B_DQS_P<2>
MEM_B_DQ<52>	BC3	MDQ1_52	MDQS1_2_N	BA37	MEM_B_DQS_N<2>
MEM_B_DQ<51>	AW4	MDQ1_51	MDQS1_1_P	BA43	MEM_B_DQS_P<1>
MEM_B_DQ<50>	AW3	MDQ1_50	MDQS1_1_N	AY42	MEM_B_DQS_N<1>
MEM_B_DQ<49>	BA3	MDQ1_49	MDQS1_0_P	AT42	MEM_B_DQS_P<0>
MEM_B_DQ<48>	BB2	MDQ1_48	MDQS1_0_N	AT43	MEM_B_DQS_N<0>
MEM_B_DQ<47>	BB5	MDQ1_47			
MEM_B_DQ<46>	BA5	MDQ1_46			
MEM_B_DQ<45>	BA8	MDQ1_45			
MEM_B_DQ<44>	BC8	MDQ1_44			
MEM_B_DQ<43>	BB4	MDQ1_43			
MEM_B_DQ<42>	BC4	MDQ1_42	MRAS1#	AW16	MEM_B_RAS_L
MEM_B_DQ<41>	BA7	MDQ1_41	MCAS1#	BA15	MEM_B_CAS_L
MEM_B_DQ<40>	AY8	MDQ1_40	MWE1#	BA16	MEM_B_WE_L
MEM_B_DQ<39>	BA9	MDQ1_39			
MEM_B_DQ<38>	BB10	MDQ1_38			
MEM_B_DQ<37>	BB12	MDQ1_37			
MEM_B_DQ<36>	AW12	MDQ1_36			
MEM_B_DQ<35>	BB8	MDQ1_35			
MEM_B_DQ<34>	BB9	MDQ1_34	MBA1_2	BB29	MEM_B_BA<2>
MEM_B_DQ<33>	AY12	MDQ1_33	MBA1_1	BB18	MEM_B_BA<1>
MEM_B_DQ<32>	BA12	MDQ1_32	MBA1_0	BB17	MEM_B_BA<0>
MEM_B_DQ<31>	BC32	MDQ1_31			
MEM_B_DQ<30>	AW32	MDQ1_30			
MEM_B_DQ<29>	BA35	MDQ1_29			
MEM_B_DQ<28>	AY36	MDQ1_28			
MEM_B_DQ<27>	BA32	MDQ1_27			
MEM_B_DQ<26>	BB32	MDQ1_26	MA1_14	BA29	MEM_B_A<14>
MEM_B_DQ<25>	BA34	MDQ1_25	MA1_13	BA14	MEM_B_A<13>
MEM_B_DQ<24>	AY35	MDQ1_24	MA1_12	AW28	MEM_B_A<12>
MEM_B_DQ<23>	BC36	MDQ1_23	MA1_11	BC28	MEM_B_A<11>
MEM_B_DQ<22>	AW36	MDQ1_22	MA1_10	BA17	MEM_B_A<10>
MEM_B_DQ<21>	BA39	MDQ1_21	MA1_9	BB28	MEM_B_A<9>
MEM_B_DQ<20>	AY40	MDQ1_20	MA1_8	AY28	MEM_B_A<8>
MEM_B_DQ<19>	BA36	MDQ1_19	MA1_7	BA28	MEM_B_A<7>
MEM_B_DQ<18>	BB36	MDQ1_18	MA1_6	AY27	MEM_B_A<6>
MEM_B_DQ<17>	BA38	MDQ1_17	MA1_5	BA27	MEM_B_A<5>
MEM_B_DQ<16>	AY39	MDQ1_16	MA1_4	BA26	MEM_B_A<4>
MEM_B_DQ<15>	BB40	MDQ1_15	MA1_3	BB26	MEM_B_A<3>
MEM_B_DQ<14>	AW40	MDQ1_14	MA1_2	BA25	MEM_B_A<2>
MEM_B_DQ<13>	AV42	MDQ1_13	MA1_1	BB25	MEM_B_A<1>
MEM_B_DQ<12>	AV41	MDQ1_12	MA1_0	BA18	MEM_B_A<0>
MEM_B_DQ<11>	BA40	MDQ1_11			
MEM_B_DQ<10>	BC40	MDQ1_10			
MEM_B_DQ<9>	AW42	MDQ1_9			
MEM_B_DQ<8>	AW41	MDQ1_8			
MEM_B_DQ<7>	AT40	MDQ1_7			
MEM_B_DQ<6>	AT41	MDQ1_6			
MEM_B_DQ<5>	AP41	MDQ1_5			
MEM_B_DQ<4>	AN40	MDQ1_4			
MEM_B_DQ<3>	AU40	MDQ1_3			
MEM_B_DQ<2>	AU41	MDQ1_2			
MEM_B_DQ<1>	AR41	MDQ1_1			
MEM_B_DQ<0>	AP42	MDQ1_0			
MEM_B_DM<7>	AT5	MDQM1_7			
MEM_B_DM<6>	BA2	MDQM1_6			
MEM_B_DM<5>	AY7	MDQM1_5			
MEM_B_DM<4>	BA11	MDQM1_4			
MEM_B_DM<3>	BB34	MDQM1_3			
MEM_B_DM<2>	BB38	MDQM1_2			
MEM_B_DM<1>	AY43	MDQM1_1			
MEM_B_DM<0>	AR42	MDQM1_0			

MEMORY CONTROL 1A

MCLK1A_2_P	BA42	TP_MEM_B_CLK2P
MCLK1A_2_N	BB42	TP_MEM_B_CLK2N
MCLK1A_1_P	BB22	MEM_B_CLK_P<1>
MCLK1A_1_N	BA22	MEM_B_CLK_N<1>
MCLK1A_0_P	BA19	MEM_B_CLK_P<0>
MCLK1A_0_N	AY19	MEM_B_CLK_N<0>
MCS1A_1#	BB14	MEM_B_CS_L<1>
MCS1A_0#	BB16	MEM_B_CS_L<0>
MODT1A_1	BB13	MEM_B_ODT<1>
MODT1A_0	AY15	MEM_B_ODT<0>
MCKE1A_1	AY31	MEM_B_CKE<1>
MCKE1A_0	BB30	MEM_B_CKE<0>

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MCP Memory Interface

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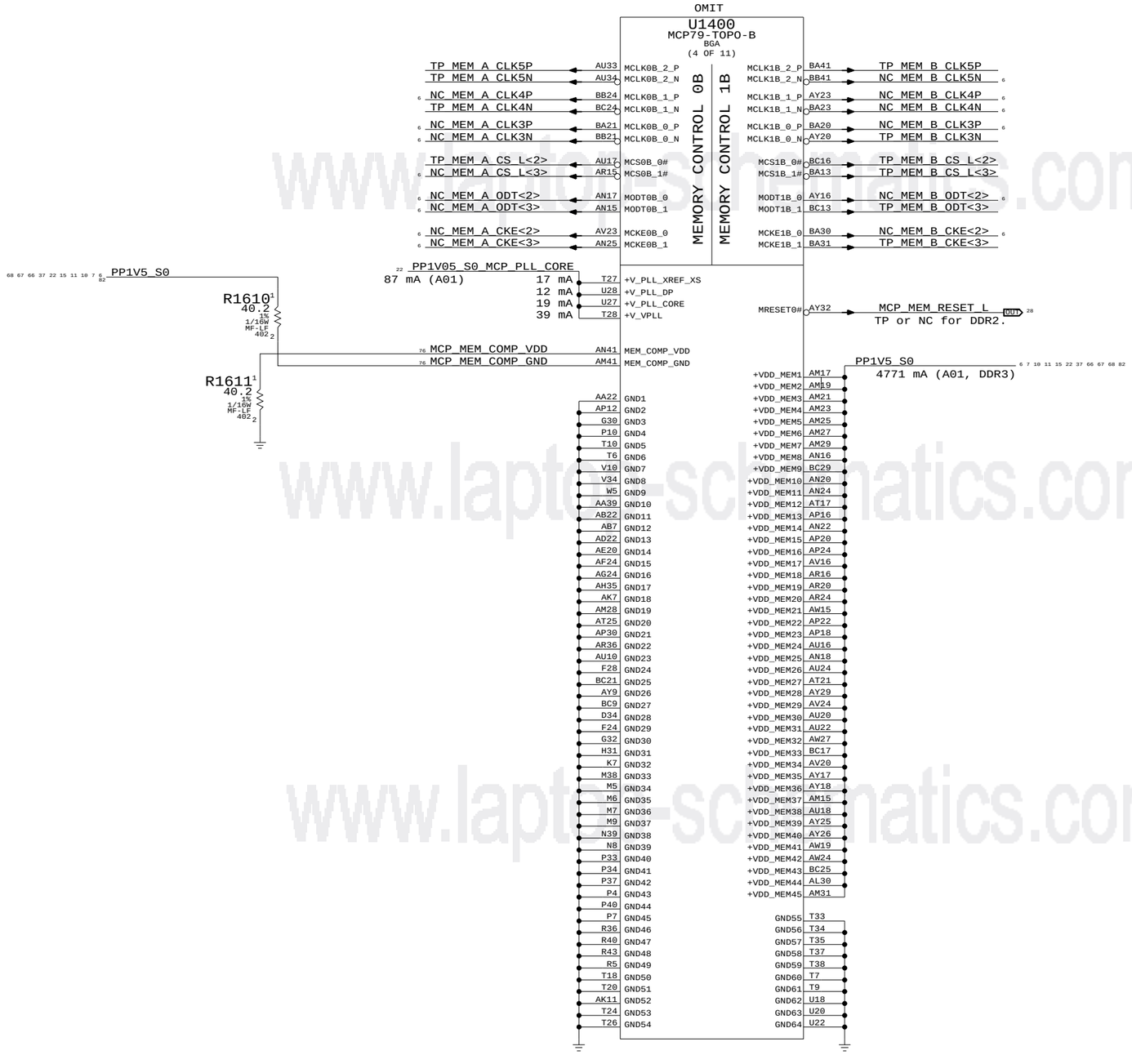

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Memory Misc		
SYNC_MASTER=T18_MLB	SYNC_DATE=02/05/2009	

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PCI EXPRESS

NC_PEG_D2RP<0>	F7	PE0_RX0_P	PE0_TX0_P	C5	NC_PEG_R2DCP<0>
NC_PEG_D2RN<0>	E7	PE0_RX0_N	PE0_TX0_N	D4	NC_PEG_R2DCN<0>
NC_PEG_D2RP<1>	D7	PE0_RX1_P	PE0_TX1_P	C4	NC_PEG_R2DCP<1>
NC_PEG_D2RN<1>	C7	PE0_RX1_N	PE0_TX1_N	B4	NC_PEG_R2DCN<1>
NC_PEG_D2RP<2>	E6	PE0_RX2_P	PE0_TX2_P	A4	NC_PEG_R2DCP<2>
NC_PEG_D2RN<2>	F6	PE0_RX2_N	PE0_TX2_N	A3	NC_PEG_R2DCN<2>
NC_PEG_D2RP<3>	E5	PE0_RX3_P	PE0_TX3_P	B3	NC_PEG_R2DCP<3>
NC_PEG_D2RN<3>	F5	PE0_RX3_N	PE0_TX3_N	B2	NC_PEG_R2DCN<3>
NC_PEG_D2RP<4>	E4	PE0_RX4_P	PE0_TX4_P	C1	NC_PEG_R2DCP<4>
NC_PEG_D2RN<4>	E3	PE0_RX4_N	PE0_TX4_N	D1	NC_PEG_R2DCN<4>
NC_PEG_D2RP<5>	C3	PE0_RX5_P	PE0_TX5_P	D2	NC_PEG_R2DCP<5>
NC_PEG_D2RN<5>	D3	PE0_RX5_N	PE0_TX5_N	E1	NC_PEG_R2DCN<5>
NC_PEG_D2RP<6>	G5	PE0_RX6_P	PE0_TX6_P	E2	NC_PEG_R2DCP<6>
NC_PEG_D2RN<6>	H5	PE0_RX6_N	PE0_TX6_N	F2	NC_PEG_R2DCN<6>
NC_PEG_D2RP<7>	J7	PE0_RX7_P	PE0_TX7_P	F3	NC_PEG_R2DCP<7>
NC_PEG_D2RN<7>	J6	PE0_RX7_N	PE0_TX7_N	F4	NC_PEG_R2DCN<7>
NC_PEG_D2RP<8>	J5	PE0_RX8_P	PE0_TX8_P	G3	NC_PEG_R2DCP<8>
NC_PEG_D2RN<8>	J4	PE0_RX8_N	PE0_TX8_N	H4	NC_PEG_R2DCN<8>
NC_PEG_D2RP<9>	L11	PE0_RX9_P	PE0_TX9_P	H3	NC_PEG_R2DCP<9>
NC_PEG_D2RN<9>	L10	PE0_RX9_N	PE0_TX9_N	H2	NC_PEG_R2DCN<9>
NC_PEG_D2RP<10>	L9	PE0_RX10_P	PE0_TX10_P	H1	NC_PEG_R2DCP<10>
NC_PEG_D2RN<10>	L8	PE0_RX10_N	PE0_TX10_N	J1	NC_PEG_R2DCN<10>
NC_PEG_D2RP<11>	L7	PE0_RX11_P	PE0_TX11_P	J2	NC_PEG_R2DCP<11>
NC_PEG_D2RN<11>	L6	PE0_RX11_N	PE0_TX11_N	J3	NC_PEG_R2DCN<11>
NC_PEG_D2RP<12>	N11	PE0_RX12_P	PE0_TX12_P	K2	NC_PEG_R2DCP<12>
NC_PEG_D2RN<12>	N10	PE0_RX12_N	PE0_TX12_N	K3	NC_PEG_R2DCN<12>
NC_PEG_D2RP<13>	N9	PE0_RX13_P	PE0_TX13_P	L4	NC_PEG_R2DCP<13>
NC_PEG_D2RN<13>	P9	PE0_RX13_N	PE0_TX13_N	L3	NC_PEG_R2DCN<13>
NC_PEG_D2RP<14>	N7	PE0_RX14_P	PE0_TX14_P	M4	NC_PEG_R2DCP<14>
NC_PEG_D2RN<14>	N6	PE0_RX14_N	PE0_TX14_N	M3	NC_PEG_R2DCN<14>
NC_PEG_D2RP<15>	N5	PE0_RX15_P	PE0_TX15_P	M2	NC_PEG_R2DCP<15>
NC_PEG_D2RN<15>	N4	PE0_RX15_N	PE0_TX15_N	M1	NC_PEG_R2DCN<15>

			PE0_REFCLK_P	E11	NC_PEG_CLK100MP
			PE0_REFCLK_N	D11	NC_PEG_CLK100MN
TP_PEG_PRSNT_L	C9	PE0_PRSNT_16# Int PU			
MINI_CLKREQ_L	D5	PEB_CLKREQ#/GPIO_49 Int PU	PE1_REFCLK_P	G11	PCIE_CLK100M_MINI_P
PCIE_MINI_PRSNT_L	D9	PEB_PRSNT# Int PU	PE1_REFCLK_N	F11	PCIE_CLK100M_MINI_N
FW_CLKREQ_L	E8	PEC_CLKREQ#/GPIO_50 Int PU	PE2_REFCLK_P	J11	PCIE_CLK100M_FW_P
PCIE_FW_PRSNT_L	C10	PEC_PRSNT# Int PU	PE2_REFCLK_N	J10	PCIE_CLK100M_FW_N
TP_EXCARD_CLKREQ_L	M15	PED_CLKREQ#/GPIO_51 Int PU	PE3_REFCLK_P	G13	NC_PCIE_CLK100M_EXCARDP
TP_PCIE_EXCARD_PRSNT_L	B10	PED_PRSNT# Int PU	PE3_REFCLK_N	F13	NC_PCIE_CLK100M_EXCARDN
TP_PE4_CLKREQ_L	L16	PEE_CLKREQ#/GPIO_16 Int PU	PE4_REFCLK_P	J13	NC_PCIE_CLK100M_PE4P
NC_PE4_PRSNT_L	L18	PEE_PRSNT#/GPIO_46 Int PU	PE4_REFCLK_N	H13	NC_PCIE_CLK100M_PE4N
AUD_IP_PERIPHERAL_DET	M16	PEF_CLKREQ#/GPIO_17 Int PU	PE5_REFCLK_P	L14	NC_PCIE_CLK100M_PE5P
TP_GMUX_JTAG_TCK_L	M18	PEF_PRSNT#/GPIO_47 Int PU	PE5_REFCLK_N	K14	NC_PCIE_CLK100M_PE5N
CARDREADER_RESET	M17	PEG_CLKREQ#/GPIO_18 Int PU	PE6_REFCLK_P	N14	NC_PCIE_CLK100M_PE6P
TP_GMUX_JTAG_TDO	M19	PEG_PRSNT#/GPIO_48 Int PU	PE6_REFCLK_N	M14	TP_PCIE_CLK100M_PE6N
PCIE_WAKE_L	F17	PE_WAKE# Int PU (S5)	PEX_RST0#	K11	PCIE_RESET_L
PCIE_MINI_D2R_P	K9	PE1_RX0_P	PE1_TX0_P	D8	PCIE_MINI_R2D_C_P
PCIE_MINI_D2R_N	J9	PE1_RX0_N	PE1_TX0_N	C8	PCIE_MINI_R2D_C_N
PCIE_FW_D2R_P	H9	PE1_RX1_P	PE1_TX1_P	B8	PCIE_FW_R2D_C_P
PCIE_FW_D2R_N	G9	PE1_RX1_N	PE1_TX1_N	A8	PCIE_FW_R2D_C_N
NC_PCIE_EXCARD_D2RP	F9	PE1_RX2_P	PE1_TX2_P	A7	NC_PCIE_EXCARD_R2DCP
NC_PCIE_EXCARD_D2RN	E9	PE1_RX2_N	PE1_TX2_N	B7	NC_PCIE_EXCARD_R2DCN
TP_PCIE_PE4_D2RP	H7	PE1_RX3_P	PE1_TX3_P	B6	TP_PCIE_PE4_R2D_CP
NC_PCIE_PE4_D2RN	G7	PE1_RX3_N	PE1_TX3_N	C6	NC_PCIE_PE4_R2D_CN

GND
57 mA (A01, DVDD0 & 1)
Minimum 1.025V for Gen2 support

	T17	+DVDD0_PEX1
	W19	+DVDD0_PEX2
	U17	+DVDD0_PEX3
	V19	+DVDD0_PEX4
	W16	+DVDD0_PEX5
	W17	+DVDD0_PEX6
	W18	+DVDD0_PEX7
	U16	+DVDD0_PEX8
PP1V05_S0	T19	+DVDD1_PEX1
	U19	+DVDD1_PEX2
PP1V05_S0_MCP_PLL_PEX 84 mA (A01)	T16	+V_PLL_PEX
MCP_PEX_CLK_COMP	A11	PEX_CLK_COMP

NO STUFF
R1710
2.37K
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 12.7mm of U1400

GND
206 mA (A01, AVDD0 & 1)
Minimum 1.025V for Gen2 support

	Y12	+AVDD0_PEX1
	AA12	+AVDD0_PEX2
	AB12	+AVDD0_PEX3
	M12	+AVDD0_PEX4
	P12	+AVDD0_PEX5
	R12	+AVDD0_PEX6
	N12	+AVDD0_PEX7
	T12	+AVDD0_PEX8
	U12	+AVDD0_PEX9
	AC12	+AVDD0_PEX10
	AD12	+AVDD0_PEX11
	V12	+AVDD0_PEX12
	W12	+AVDD0_PEX13
PP1V05_S0_MCP_PEX_AVDD	M13	+AVDD1_PEX1
	N13	+AVDD1_PEX2
	P13	+AVDD1_PEX3

If PE0 interface is not used, ground DVDD0_PEX and AVDD0_PEX.
If PE1 interface is not used, ground DVDD1_PEX and AVDD1_PEX.

MCP PCIe Interfaces

SYNC_MASTER=T18_MLB SYNC_DATE=02/05/2009

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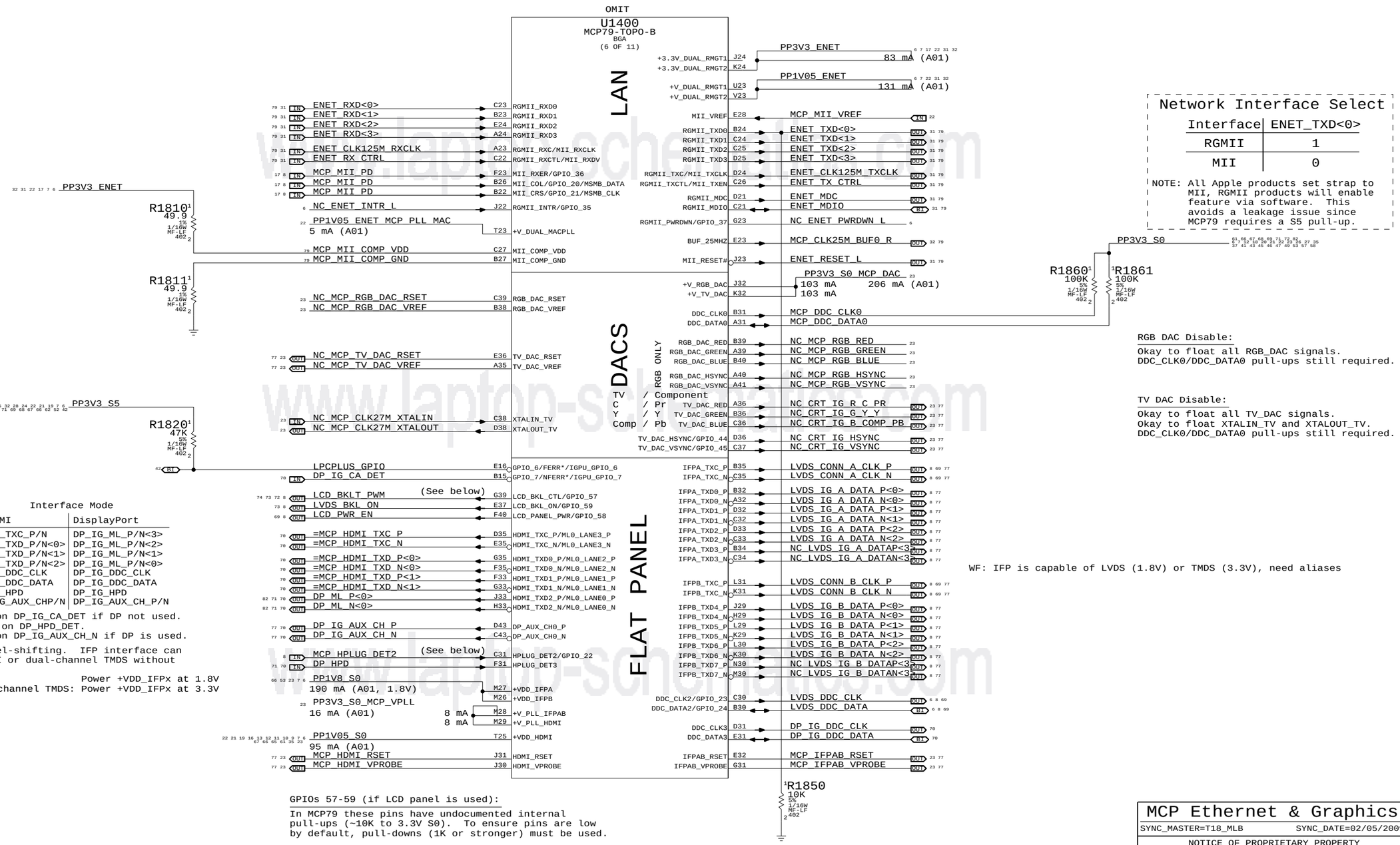

Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.
LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

MCP Ethernet & Graphics

SYNC_MASTER=T18_MLB SYNC_DATE=02/05/2009

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MCP79-TOPO-B
BGA
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PCI

PCI_REQ0 L	T2	PCI_REQ0#	PCI_GNT0#	R3	NC_PCI_GNT0_L
PCI_REQ1 L	V9	PCI_REQ1#/FANRPM2	PCI_GNT1#/FANCTL2	U10	NC_PCI_GNT1_L
FW_PWR_EN	T3	PCI_REQ2#/GPIO_40/RS232_DSR#	PCI_GNT2#/GPIO_41/RS232_DTR#	R4	TP_GMUX_JTAG_TMS
AUD_IPHS_SWITCH_EN	U9	PCI_REQ3#/GPIO_38/RS232_CTS#	PCI_GNT3#/GPIO_39/RS232_RTS#	U11	TP_GMUX_JTAG_TDI
MCP_RS232_SIN_L	T4	PCI_REQ4#/GPIO_52/RS232_SIN#	PCI_GNT4#/GPIO_53/RS232_SOUT#	P3	MCP_RS232_SOUT_L
MCP_DEBUG<0>	AC3	PCI_AD0	PCI_CBE0#	AA3	NC_PCI_C_BE_L<0>
MCP_DEBUG<1>	AE10	PCI_AD1	PCI_CBE1#	AA6	NC_PCI_C_BE_L<1>
MCP_DEBUG<2>	AC4	PCI_AD2	PCI_CBE2#	AA11	NC_PCI_C_BE_L<2>
MCP_DEBUG<3>	AE11	PCI_AD3	PCI_CBE3#	W10	NC_PCI_C_BE_L<3>
MCP_DEBUG<4>	AB3	PCI_AD4	PCI_DEVSEL#	AA9	NC_PCI_DEVSEL_L
MCP_DEBUG<5>	AC6	PCI_AD5	PCI_FRAME#	Y4	NC_PCI_FRAME_L
MCP_DEBUG<6>	AB2	PCI_AD6	PCI_IRDY#	AA10	NC_PCI_IRDY_L
MCP_DEBUG<7>	AC7	PCI_AD7	PCI_PAR	Y1	TP_PCI_PAR
NC_PCI_AD<8>	AC8	PCI_AD8	PCI_PERR#/GPIO_43/RS232_DCD#	AB9	NC_PCI_PERR_L
NC_PCI_AD<9>	AA2	PCI_AD9	PCI_SERR#	AA7	NC_PCI_SERR_L
NC_PCI_AD<10>	AC9	PCI_AD10	PCI_STOP#	Y2	NC_PCI_STOP_L
NC_PCI_AD<11>	AC10	PCI_AD11	PCI_PME#/GPIO_30 Int PU (S5)	T1	PM_LATRIGGER_L
NC_PCI_AD<12>	AC11	PCI_AD12	PCI_RESET0#	R10	MEM_VTT_EN_R
NC_PCI_AD<13>	AA1	PCI_AD13	PCI_RESET1#	R11	NC_PCI_RESET1_L
NC_PCI_AD<14>	AA5	PCI_AD14	PCI_CLK0	R6	NC_PCI_CLK0
NC_PCI_AD<15>	Y5	PCI_AD15	PCI_CLK1	R7	NC_PCI_CLK1
NC_PCI_AD<16>	W3	PCI_AD16	PCI_CLK2	R8	PCI_CLK33M_MCP_R
NC_PCI_AD<17>	W6	PCI_AD17	PCI_CLKIN	R9	PCI_CLK33M_MCP
NC_PCI_AD<18>	W4	PCI_AD18			
NC_PCI_AD<19>	W7	PCI_AD19			
NC_PCI_AD<20>	V3	PCI_AD20			
NC_PCI_AD<21>	W8	PCI_AD21			
NC_PCI_AD<22>	V2	PCI_AD22			
NC_PCI_AD<23>	W9	PCI_AD23			
NC_PCI_AD<24>	U3	PCI_AD24			
NC_PCI_AD<25>	W11	PCI_AD25			
NC_PCI_AD<26>	U2	PCI_AD26			
NC_PCI_AD<27>	U5	PCI_AD27			
NC_PCI_AD<28>	U1	PCI_AD28			
NC_PCI_AD<29>	U6	PCI_AD29			
NC_PCI_AD<30>	T5	PCI_AD30			
NC_PCI_AD<31>	U7	PCI_AD31			

R1910
22
5% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to pin R8

LPC

NC_PCI_INTW_L	P2	PCI_INTW#	LPC_FRAME#	AD4	LPC_FRAME_R_L R1960 22 5% 1/16W MF-LF 402 LPC_FRAME_L
NC_PCI_INTX_L	N3	PCI_INTX#	LPC_PWRDWN#/GPIO_54/EXT_NMI#	AE12	LPC_PWRDWN_L
TP_PCI_INTY_L	N2	PCI_INTY#	LPC_RESET0#	AE5	LPC_RESET_L
NC_PCI_INTZ_L	N1	PCI_INTZ#	LPC_AD0	AD3	LPC_AD_R<0> R1950 22 5% 1/16W MF-LF 402 LPC_AD<0>
NC_PCI_TRDY_L	Y3	PCI_TRDY#	LPC_AD1	AD2	LPC_AD_R<1> R1951 22 5% 1/16W MF-LF 402 LPC_AD<1>
PM_CLKRUN_L	AD11	PCI_CLKRUN#/GPIO_42	LPC_AD2	AD1	LPC_AD_R<2> R1952 22 5% 1/16W MF-LF 402 LPC_AD<2>
FW_PLUG_DET_L	AE2	LPC_DRQ1#/GPIO_19 Int PU	LPC_AD3	AD5	LPC_AD_R<3> R1953 22 5% 1/16W MF-LF 402 LPC_AD<3>
NC_LPC_DRQ0_L	AE1	LPC_DRQ0# Int PU	LPC_CLK0	AE9	LPC_CLK33M_SMC_R
LPC_SERIRQ	AE6	LPC_SERIRQ Int PU			

R1961
10K
5% 1/16W MF-LF 402
Strap for Boot ROM Selection (See HDA_SDOUT)

GND

U24	GND65	GND98	Y26
U26	GND66	GND99	Y27
U39	GND67	GND100	AB18
U4	GND68	GND101	H34
U8	GND69	GND102	AB20
V16	GND70	GND103	AB21
V17	GND71	GND104	AB23
V18	GND72	GND105	AB24
V20	GND73	GND106	AB25
V22	GND74	GND107	AB26
V24	GND75	GND108	AB27
V26	GND76	GND109	AB28
V27	GND77	GND110	AB34
V28	GND78	GND111	AB37
V33	GND79	GND112	AB4
V37	GND80	GND113	AB40
V4	GND81	GND114	AC22
V40	GND82	GND115	AC36
V7	GND83	GND116	AC40
W20	GND84	GND117	AB33
W22	GND85	GND118	AC5
W24	GND86	GND119	AD16
W36	GND87	GND120	AD17
W40	GND88	GND121	AD18
W43	GND89	GND122	AD19
Y16	GND90	GND123	AD20
Y17	GND91	GND124	AD24
Y18	GND92	GND125	AD25
Y19	GND93	GND126	AD26
Y20	GND94	GND127	AD27
Y22	GND95	GND128	AD28
Y24	GND96	GND129	AD33
Y25	GND97	GND130	AD34

PP3V3_S0

MCP_RS232_SOUT_L	R1989	8.2K 5% 1/16W MF-LF 402
PCI_REQ0_L	R1990	8.2K 5% 1/16W MF-LF 402
PCI_REQ1_L	R1991	8.2K 5% 1/16W MF-LF 402
FW_PWR_EN	R1992	8.2K 5% 1/16W MF-LF 402
MCP_RS232_SIN_L	R1994	8.2K 5% 1/16W MF-LF 402

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MCP PCI & LPC

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SATA

77 37 OUT	SATA_HDD_R2D_C_P	AJ7	SATA_A0_TX_P
77 37 OUT	SATA_HDD_R2D_C_N	AJ6	SATA_A0_TX_N
77 37 IN	SATA_HDD_D2R_N	AJ5	SATA_A0_RX_N
77 37 IN	SATA_HDD_D2R_P	AJ4	SATA_A0_RX_P
77 37 OUT	SATA_ODD_R2D_C_P	AJ11	SATA_A1_TX_P
77 37 OUT	SATA_ODD_R2D_C_N	AJ10	SATA_A1_TX_N
77 37 IN	SATA_ODD_D2R_N	AJ9	SATA_A1_RX_N
77 37 IN	SATA_ODD_D2R_P	AK9	SATA_A1_RX_P
6	NC_SATA_C_R2D_CP	AK2	SATA_B0_TX_P
6	NC_SATA_C_R2D_CN	AJ3	SATA_B0_TX_N
	TP_SATA_C_D2RN	AJ2	SATA_B0_RX_N
6	NC_SATA_C_D2RP	AJ1	SATA_B0_RX_P
	TP_SATA_D_R2D_CP	AM4	SATA_B1_TX_P
	TP_SATA_D_R2D_CN	AL3	SATA_B1_TX_N
6	NC_SATA_D_D2RN	AL4	SATA_B1_RX_N
6	NC_SATA_D_D2RP	AK3	SATA_B1_RX_P
	TP_SATA_E_R2D_CP	AN1	SATA_C0_TX_P
	TP_SATA_E_R2D_CN	AM1	SATA_C0_TX_N
	TP_SATA_E_D2RN	AM2	SATA_C0_RX_N
	TP_SATA_E_D2RP	AM3	SATA_C0_RX_P
	TP_SATA_F_R2D_CP	AP3	SATA_C1_TX_P
	TP_SATA_F_R2D_CN	AP2	SATA_C1_TX_N
	TP_SATA_F_D2RN	AN3	SATA_C1_RX_N
	TP_SATA_F_D2RP	AN2	SATA_C1_RX_P
	TP_MCP_SATALED_L	E12	SATA_LED#
22	PP1V05_S0_MCP_PLL_SATA	AE16	+V_PLL_SATA
	84 mA (A01)		
22 21 17 16 13 12 11 10 9 7 6 67 66 65 61 35 23	PP1V05_S0		
	43 mA (A01, DVDD0 & 1)	AF19	+DVDD0_SATA1
	Minimum 1.025V for Gen2 support	AG16	+DVDD0_SATA2
		AG17	+DVDD0_SATA3
		AG19	+DVDD0_SATA4
	GND	AH17	+DVDD1_SATA1
		AH19	+DVDD1_SATA2
22 7	PP1V05_S0_MCP_SATA_AVDD		
	127 mA (A01, AVDD0 & 1)	AJ12	+AVDD0_SATA1
	Minimum 1.025V for Gen2 support	AN11	+AVDD0_SATA2
		AK12	+AVDD0_SATA3
		AK13	+AVDD0_SATA4
		AL12	+AVDD0_SATA5
		AM11	+AVDD0_SATA6
		AM12	+AVDD0_SATA7
		AN12	+AVDD0_SATA8
		AL13	+AVDD0_SATA9
	GND	AN14	+AVDD1_SATA1
		AL14	+AVDD1_SATA2
		AM13	+AVDD1_SATA3
		AM14	+AVDD1_SATA4
77	MCP_SATA_TERMP	AE3	SATA_TERMP

R2010 1 2.49K 1% 1/16W MF-LF 402 2

If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

USB

External A
USB0_P	C29	USB_EXTA_P	B1 38 78
USB0_N	D29	USB_EXTA_N	B1 38 78

AirPort (PCIe Mini-Card)
USB1_P	C28	NC_USB_MINIP	B1 8 78
USB1_N	D28	NC_USB_MININ	B1 8 78

External D
USB2_P	A28	NC_USB_EXTDP	B1 8 78
USB2_N	B28	NC_USB_EXTDN	B1 8 78

Camera
USB3_P	F29	USB_CAMERA_P	B1 6 29 78
USB3_N	G29	USB_CAMERA_N	B1 6 29 78

IR
USB4_P	K27	USB_IR_P	B1 39 78
USB4_N	L27	USB_IR_N	B1 39 78

Geyser Trackpad/Keyboard
USB5_P	J26	USB_TPAD_P	B1 48 78
USB5_N	J27	USB_TPAD_N	B1 48 78

Bluetooth
USB6_P	F27	USB_BT_P	B1 6 29 78
USB6_N	G27	USB_BT_N	B1 6 29 78

External B
USB7_P	D27	USB_EXTB_P	B1 38 78
USB7_N	E27	USB_EXTB_N	B1 38 78

ExpressCard
USB8_P	K25	NC_USB_EXCARDP	B1 8 78
USB8_N	L25	NC_USB_EXCARDN	B1 8 78

External C
USB9_P	H25	NC_USB_EXTCP	B1 8 78
USB9_N	J25	NC_USB_EXTCN	B1 8 78
USB10_P	F25	NC_USB_10P	6
USB10_N	G25	NC_USB_10N	6

SD Card Reader
USB11_P	K23	USB_CARDREADER_P	B1 30 78
USB11_N	L23	USB_CARDREADER_N	B1 30 78

USB_OC0#/GPIO_25	L21	USB_EXTA_OC_L	38
USB_OC1#/GPIO_26	K21	USB_EXTB_OC_L	38
USB_OC2#/GPIO_27/MGPIO	J21	USB_EXTC_OC_L	
USB_OC3#/GPIO_28/MGPIO	H21	EXCARD_OC_L	

PP3V3_S5 5 7 17 21 22 24 28 33 35 36 42 52 63 66 67 68 69 71 82

R2051 1 8.2K 5% 1/16W MF-LF 402 2
R2053 1 8.2K 5% 1/16W MF-LF 402 2
R2050 1 8.2K 5% 1/16W MF-LF 402 2
R2052 1 8.2K 5% 1/16W MF-LF 402 2

+V_PLL_USB	L28	PP3V3_S0_MCP_PLL_USB	22
		19 mA (A01)	
USB_RBIAS_GND	A27	78 MCP_USB_RBIAS_GND	

R2060 1 806 1% 1/10W MF-LF 402 2

GND131	AD35	GND145	AF27
GND132	AD37	GND146	AF28
GND133	AD38	GND147	AF33
GND134	AE22	GND148	AF34
GND135	AE24	GND149	AF37
GND136	AE39	GND150	AF40
GND137	AE4	GND151	AG18
GND138	AD6	GND152	AG20
GND139	AF16	GND153	AG22
GND140	AF17	GND154	AG26
GND141	AF18	GND155	AG36
GND142	AF20	GND156	AG40
GND143	AF22	GND157	AH18
GND144	AF26	GND158	AH20
		GND159	AH22
		GND160	AH24

MCP SATA & USB

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HDA

HDA_SDIN0 — G15 HDA_SDATA_IN0 — Int PD
NC_MLB_RAM_SIZE — J14 HDA_SDATA_IN1_GPIO_2/PS2_KB_CLK — Int PD
TP_MLB_RAM_VENDOR (MXM_OK for MXM systems) — J15 HDA_SDATA_IN2_GPIO_3/PS2_KB_DATA — Int PD

PP3V3_S0 — R2110 49.9 1% 1/16W MF-LF 402 — MCP_HDA_PULLDN_COMP — A15 HDA_PULLDN_COMP

PP1V05_S0_MCP_PLL_NV — 37 mA (A01) — 20 mA / 17 mA — AE18 +V_PLL_NV_H, AE17 +V_PLL_SP_SPREF

PP3V42_G3H — R2120 49.9K 1% 1/16W MF-LF 402 — R2121 49.9K 1% 1/16W MF-LF 402

SPIROM_USE_MLB — L24 GPIO_1/PWRDN_OK/SPI_CS1
SMC_ADAPTER_EN — L26 GPIO_12_SUS_STAT_ACCLMTR_EXT_TRIG_L
NC_SB_A20GATE — K13 A20GATE — Int PU
TP_MCP_KBDRSTIN_L — L13 KBRDRSTIN* — Int PU
SMC_WAKE_SCI_L — C19 SIO_PME* — Int PU (S5)
SMC_RUNTIME_SCI_L — C18 EXT_SMI/GPIO_32* — Int PU (S5)
SM_INTRUDER_L — B20 INTRUDER*
TP_MCP_LID_L — M25 LID* — Int PU (S5)
PM_BATLOW_L — M24 LLB* — Int PU (S5)
PM_DPRSLPVR — M22 CPU_DPRSLPVR
PM_PWRBTN_L — C16 PWRBTN* — Int PU (S5)
PM_SYSRST_DEBOUNCE_L — D16 RSTBTN* — Int PU
RTC_RST_L — C20 RTC_RST*
PM_RSMRST_L — D20 PWRGD_SB
MCP_PS_PWRGD — E20 PS_PWRGD
MCP_CPU_VLD — C17 CPU_VLD
JTAG_MCP_TDI — E19 JTAG_TDI — Int PU
JTAG_MCP_TDO — F19 JTAG_TDO
JTAG_MCP_TMS — J19 JTAG_TMS — Int PU
JTAG_MCP_TRST_L — J18 JTAG_TRST*
JTAG_MCP_TCK — G19 JTAG_TCK
MCP_CLK25M_XTALIN — A16 XTALIN
MCP_CLK25M_XTALOUT — B16 XTALOUT
RTC_CLK32K_XTALIN — A19 XTALIN_RTC
RTC_CLK32K_XTALOUT — B19 XTALOUT_RTC

R2150 10K 5% 1/16W MF-LF 402
R2151 100K 5% 1/16W MF-LF 402

PP3V3_S0 — R2160 8.2K 5% 1/16W MF-LF 402 — 7 mA (A01)

+V_DUAL_HDA1 J16, +V_DUAL_HDA2 K16

HDA_SDATA_OUT F15 — HDA_SDOUT_R — R2170 22 5% 1/16W MF-LF 402 — HDA_SDOUT
HDA_BITCLK E15 — HDA_BIT_CLK_R — R2171 22 5% 1/16W MF-LF 402 — HDA_BIT_CLK
HDA_RESET* K15 — HDA_RST_R_L — R2172 22 5% 1/16W MF-LF 402 — HDA_RST_L
HDA_SYNC L15 — HDA_SYNC_R — R2173 22 5% 1/16W MF-LF 402 — HDA_SYNC

HDA_DOCK_EN*_GPIO_4/PS2_MS_CLK K17 — MCP_GPIO_4
HDA_DOCK_RST*_GPIO_5/PS2_MS_DATA L17 — AUD_I2C_INT_L

SLP_S3* G17 — PM_SLP_S3_L
SLP_RMGT* J17 — PM_SLP_RMGT_L
SLP_S5* H17 — PM_SLP_S4_L

THERM_DIODE_P B11 — MCP_THMDIODE_P
THERM_DIODE_N C11 — MCP_THMDIODE_N

MCP_VID0/GPIO_13 L20 — MCP_VID<0>
MCP_VID1/GPIO_14 M20 — MCP_VID<1>
MCP_VID2/GPIO_15 M21 — MCP_VID<2>

SPKR C13 — MCP_SPKR

PP3V3_S0 — R2180 10K 5% 1/16W MF-LF 402 — BOOT_MODE_SAFE
BOOT_MODE_USER — R2181 10K 5% 1/16W MF-LF 402
USER mode: Normal
SAFE mode: For ROMSIP recovery
Connects to SMC for automatic recovery.

MISC

SMB_CLK0 L19 — SMBUS_MCP_0_CLK
SMB_DATA0 K19 — SMBUS_MCP_0_DATA
SMB_CLK1/MSMB_CLK G21 — SMBUS_MCP_1_CLK
SMB_DATA1/MSMB_DATA F21 — SMBUS_MCP_1_DATA
SMB_ALERT*/GPIO_64 M23 — AP_PWR_EN

(MGPIO2) FANRPM0/GPIO_60 B12 — MEM_EVENT_L
FANCTL0/GPIO_61 A12 — ODD_PWR_EN_L
(MGPIO3) FANRPM1/GPIO_63 D12 — SMC_IG_THROTTLE_L
FANCTL1/GPIO_62 C12 — ARB_DETECT

CPUVDD_EN D17 — MCP_CPUVDD_EN

SPI_CS0/GPIO_10 C14 — SPI_CS0_R_L
SPI_CLK/GPIO_11 D13 — SPI_CLK_R
SPI_DI/GPIO_8 C15 — SPI_MISO
SPI_DO/GPIO_9 B14 — SPI_MOSI_R

SUS_CLK/GPIO_34 B18 — PM_CLK32K_SUSCLK_R
BUF_SIO_CLK AE7 — TP_MCP_BUF_SIO_CLK

TEST_MODE_EN K22 — MCP_TEST_MODE_EN
PKG_TEST L22

R2163 10K 5% 1/16W MF-LF 402
R2190 1K 1% 1/16W MF-LF 402

BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface

HDA_SDOUT_R — C2170 10PF 5% 50V CERM 402
HDA_BIT_CLK_R — C2171 10PF 5% 50V CERM 402
HDA_RST_R_L — C2172 10PF 5% 50V CERM 402
HDA_SYNC_R — C2173 10PF 5% 50V CERM 402

PP3V3_S0 — R2140 10K 5% 1/16W MF-LF 402 — R2141 10K 5% 1/16W MF-LF 402 — R2142 10K 5% 1/16W MF-LF 402 — R2143 10K 5% 1/16W MF-LF 402
MCP_GPIO_4
AUD_I2C_INT_L
MEM_EVENT_L
SMC_IG_THROTTLE_L
ARB_DETECT
R2147 100K 5% 1/16W MF-LF 402

PP3V3_S3 — R2154 100K 5% 1/16W MF-LF 402 — AP_PWR_EN

MCP_VID<0>
MCP_VID<1>
MCP_VID<2>
R2155 22K 5% 1/16W MF-LF 402
R2156 22K 5% 1/16W MF-LF 402
R2157 22K 5% 1/16W MF-LF 402

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP HDA & MISC

SYNC_MASTER=T18_MLB SYNC_DATE=02/05/2009

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7903	A

SCALE: NONE SHT 20 OF 83

OMIT

U1400
MCP79-TOPO-B
BGA
(11 OF 11)

AH26	GND161	GND253	AV40
AH33	GND162	GND254	BA1
AH34	GND163	GND255	BA4
AH37	GND164	GND256	AW31
AH38	GND165	GND257	AY6
AJ39	GND166	GND258	L35
AJ8	GND167	GND259	BC33
AK10	GND168	GND260	BC37
AK33	GND169	GND261	BC41
AK34	GND170	GND262	AY14
AK37	GND171	GND263	BC5
AK4	GND172	GND264	C2
AK40	GND173	GND265	D10
AL36	GND174	GND266	D14
AL40	GND175	GND267	D15
AL5	GND176	GND268	D18
AM10	GND177	GND269	D19
AM16	GND178	GND270	D22
AM18	GND179	GND271	D23
AM20	GND180	GND272	D26
AM22	GND181	GND273	D30
AM24	GND182	GND274	D37
AM26	GND183	GND275	D6
AM30	GND184	GND276	E13
AM34	GND185	GND277	E17
AM35	GND186	GND278	E21
AM37	GND187	GND279	E25
AM38	GND188	GND280	E29
AM5	GND189	GND281	E33
AM6	GND190	GND282	F12
AM7	GND191	GND283	F16
AM9	GND192	GND284	F32
AP26	GND193	GND285	F8
AN28	GND194	GND286	G10
AN30	GND195	GND287	G12
AN39	GND196	GND288	G14
AN4	GND197	GND289	G16
Y7	GND198	GND290	BC12
AP10	GND199	GND291	G22
AU26	GND200	GND292	G24
AP14	GND201	GND293	AW20
AU14	GND202	GND294	G34
AP28	GND203	GND295	G4
AP32	GND204	GND296	G43
AP34	GND205	GND297	G6
AP36	GND206	GND298	G8
AP37	GND207	GND299	H11
AP4	GND208	GND300	H15
AP40	GND209	GND301	AW35
AP7	GND210	GND302	H23
AW23	GND211	GND303	AN8
AR28	GND212	GND304	G40
AR32	GND213	GND305	J12
AR40	GND214	GND306	J8
AT10	GND215	GND307	K10
AR12	GND216	GND308	K12
AT13	GND217	GND309	K18
AT29	GND218	GND310	K26
AT33	GND219	GND311	K37
AT6	GND220	GND312	K4
AT7	GND221	GND313	K40
AT9	GND222	GND314	K8
AY21	GND223	GND315	AU1
AY22	GND224	GND316	L40
L12	GND225	GND317	L43
AU12	GND226	GND318	L5
AU28	GND227	GND319	M10
AP33	GND228	GND320	M34
AU32	GND229	GND321	M35
AR30	GND230	GND322	M37
AU36	GND231	GND323	Y28
AU38	GND232	GND324	Y33
AU4	GND233	GND325	Y34
G28	GND234	GND326	Y35
F20	GND235	GND327	Y37
AV28	GND236	GND328	Y38
AV32	GND237	GND329	AB17
AV36	GND238	GND330	AB16
AV4	GND239	GND331	AN26
AV7	GND240	GND332	AD7
AW11	GND241	GND333	M11
G20	GND242	GND334	AA4
AR43	GND243	GND335	AB19
AW43	GND244	GND336	AY13
AY10	GND245	GND337	P11
AV12	GND246	GND338	Y6
AY30	GND247	GND339	T11
AY33	GND248	GND340	V11
AY34	GND249	GND341	Y11
AY37	GND250	GND342	AH16
AY38	GND251	GND343	T22
AY41	GND252		

GND

PPVCORE_S0_MCP
64 44 22 7 6
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

OMIT

U1400
MCP79-TOPO-B
BGA
(10 OF 11)

AA25	+VDD_CORE1	+VTT_CPU1	R32	PP1V05_S0	1139 mA
AC23	+VDD_CORE2	+VTT_CPU2	AC32		
U25	+VDD_CORE3	+VTT_CPU3	E40		
AH12	+VDD_CORE4	+VTT_CPU4	J36		
AG10	+VDD_CORE5	+VTT_CPU5	N32		
AG5	+VDD_CORE6	+VTT_CPU6	T32		
Y21	+VDD_CORE7	+VTT_CPU7	U32		
Y23	+VDD_CORE8	+VTT_CPU8	V32		
AA16	+VDD_CORE9	+VTT_CPU9	W32		
AA26	+VDD_CORE10	+VTT_CPU10	P31		
AA27	+VDD_CORE11	+VTT_CPU11	AF32		
AA28	+VDD_CORE12	+VTT_CPU12	AE32		
AC16	+VDD_CORE13	+VTT_CPU13	AH32		
AC17	+VDD_CORE14	+VTT_CPU14	AJ32		
AC18	+VDD_CORE15	+VTT_CPU15	AK31		
AC19	+VDD_CORE16	+VTT_CPU16	AK32		
AC20	+VDD_CORE17	+VTT_CPU17	AD32		
AC21	+VDD_CORE18	+VTT_CPU18	AL31		
AA17	+VDD_CORE19	+VTT_CPU19	AB32		
AC24	+VDD_CORE20	+VTT_CPU20	B41		
AC25	+VDD_CORE21	+VTT_CPU21	B42		
AC26	+VDD_CORE22	+VTT_CPU22	C40		
AC27	+VDD_CORE23	+VTT_CPU23	C41		
AC28	+VDD_CORE24	+VTT_CPU24	C42		
AD21	+VDD_CORE25	+VTT_CPU25	D39		
AD23	+VDD_CORE26	+VTT_CPU26	D40		
W27	+VDD_CORE27	+VTT_CPU27	D41		
V25	+VDD_CORE28	+VTT_CPU28	E38		
AA18	+VDD_CORE29	+VTT_CPU29	E39		
AE19	+VDD_CORE30	+VTT_CPU30	F37		
AE21	+VDD_CORE31	+VTT_CPU31	F38		
AE23	+VDD_CORE32	+VTT_CPU32	F39		
AE25	+VDD_CORE33	+VTT_CPU33	G36		
AE26	+VDD_CORE34	+VTT_CPU34	G37		
AE27	+VDD_CORE35	+VTT_CPU35	G38		
AE28	+VDD_CORE36	+VTT_CPU36	H35		
AF10	+VDD_CORE37	+VTT_CPU37	H37		
AF11	+VDD_CORE38	+VTT_CPU38	J34		
AA19	+VDD_CORE39	+VTT_CPU39	J35		
AF2	+VDD_CORE40	+VTT_CPU40	K33		
AF21	+VDD_CORE41	+VTT_CPU41	K34		
AF23	+VDD_CORE42	+VTT_CPU42	K35		
AF25	+VDD_CORE43	+VTT_CPU43	L32		
AF3	+VDD_CORE44	+VTT_CPU44	L33		
AF4	+VDD_CORE45	+VTT_CPU45	L34		
AF7	+VDD_CORE46	+VTT_CPU46	M31		
AH23	+VDD_CORE47	+VTT_CPU47	M32		
AF9	+VDD_CORE48	+VTT_CPU48	M33		
AA20	+VDD_CORE49	+VTT_CPU49	N31		
AG11	+VDD_CORE50	+VTT_CPU50	P32		
AG12	+VDD_CORE51	+VTT_CPU51	Y32		
AG21	+VDD_CORE52	+VTT_CPU52	AA32		
AG23	+VDD_CORE53				
AG25	+VDD_CORE54	+VTT_CPUCLK	AG32	43 mA	
AG3	+VDD_CORE55				
AG4	+VDD_CORE56				
AA21	+VDD_CORE57				
AG6	+VDD_CORE58				
AG7	+VDD_CORE59	+3.3V_1	AD10	PP3V3_S0	450 mA (A01)
AG8	+VDD_CORE60	+3.3V_2	AE8		
AG9	+VDD_CORE61	+3.3V_3	AB10		
AH1	+VDD_CORE62	+3.3V_4	AD9		
AH10	+VDD_CORE63	+3.3V_5	Y10		
AH11	+VDD_CORE64	+3.3V_6	AB11		
W26	+VDD_CORE65	+3.3V_7	AA8		
AH2	+VDD_CORE66	+3.3V_8	Y9		
AA23	+VDD_CORE67				
W28	+VDD_CORE68				
AH25	+VDD_CORE69			PP3V3_S5	266 mA (A01)
AH21	+VDD_CORE70	+3.3V_DUAL1	G18	16 mA	
AH3	+VDD_CORE71	+3.3V_DUAL2	H19		
AH4	+VDD_CORE72	+3.3V_DUAL3	J20		
AH5	+VDD_CORE73	+3.3V_DUAL4	K20		
AH6	+VDD_CORE74				
AH7	+VDD_CORE75	+3.3V_DUAL_USB1	G26	250 mA	
AH9	+VDD_CORE76	+3.3V_DUAL_USB2	H27		
AA24	+VDD_CORE77	+3.3V_DUAL_USB3	J28		
W21	+VDD_CORE78	+3.3V_DUAL_USB4	K28		
W23	+VDD_CORE79				
W25	+VDD_CORE80				
AF12	+VDD_CORE81				
		+VDD_AUXC1	T21	PP1V05_S5	105 mA (A01)
		+VDD_AUXC2	U21		
A20	+VBAT	+VDD_AUXC3	V21		

POWER

PP3V42_G3H
45 43 42 41 40 39 24 20 7 6 67 60 59 48
10 uA (G3)
80 uA (S0)

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MCP Power & Ground

SYNC_MASTER=T18_MLB SYNC_DATE=02/05/2009

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE: NONE	SHT 21 OF 83	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Core Power

NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)

PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)
(No IG vs. EG data)

C2500 4.7UF 20% 4V X5R 402
C2501 4.7UF 20% 4V X5R 402
C2502 4.7UF 20% 4V X5R 402
C2503 4.7UF 20% 4V X5R 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

MCP PCIE (DVDD) Power

PP1V05_S0
57 mA (A01)

C2515 4.7UF 20% 4V X5R 402
C2516 1UF 10% 10V X5R 402-1
C2517 1UF 10% 10V X5R 402-1
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402

MCP SATA (DVDD) Power

PP1V05_S0
43 mA (A01)

C2520 4.7UF 20% 4V X5R 402
C2521 0.1UF 20% 10V CERM 402

PP1V05_S0
333 mA (A01)

L2570 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)

C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF

PP1V05_S0_MCP_PEX_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM 206 mA (A01)
VOLTAGE=1.05V

MCP 1.05V AUX Power

PP1V05_S5
105 mA (A01)

C2525 0.1uF 20% 10V CERM 402
C2526 0.1uF 20% 10V CERM 402

MCP 1.05V RMGT Power

PP1V05_ENET
131 mA (A01)

C2528 4.7UF 20% 4V X5R 402
C2529 0.1UF 20% 10V CERM 402

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

L2575 30-OHM-5A 0603

C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF

PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM 127 mA (A01)
VOLTAGE=1.05V

MCP FSB (VTT) Power

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)

PP1V05_S0
1182 mA (A01)

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

PP1V05_S0_MCP_PLL_UF
562 mA (A01)

L2580 30-OHM-1.7A 0402

C2580 4.7UF 20% 4V X5R 402
C2581 0.1UF 20% 10V CERM 402

PP1V05_S0_MCP_PLL_FSB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM 270 mA (A01)
VOLTAGE=1.05V

MCP Memory Power

PP1V5_S0
4771 mA (A01, DDR3)

C2540 4.7UF 20% 4V X5R 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

L2582 30-OHM-1.7A 0402

C2582 4.7UF 20% 4V X5R 402
C2583 0.1UF 20% 10V CERM 402

PP1V05_S0_MCP_PLL_PEX
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM 84 mA (A01)
VOLTAGE=1.05V

MCP 3.3V Power

NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)

PP3V3_S0
450 mA (A01)

C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

PP3V3_S0
19 mA (A01)

L2555 30-OHM-1.7A 0402

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

C2555 2.2UF 20% 6.3V CERM 402-LF

PP3V3_S0_MCP_PLL_USB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM 19 mA (A01)
VOLTAGE=3.3V

L2584 30-OHM-1.7A 0402

C2584 4.7UF 20% 4V X5R 402
C2585 0.1UF 20% 10V CERM 402

PP1V05_S0_MCP_PLL_SATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM 84 mA (A01)
VOLTAGE=1.05V

MCP 3.3V AUX/USB Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

PP3V3_S5
266 mA (A01)

C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V Ethernet Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

PP3V3_ENET
83 mA (A01)

C2564 2.2UF 20% 6.3V CERM 402-LF

L2586 30-OHM-1.7A 0402

C2586 4.7UF 20% 4V X5R 402
C2587 0.1UF 20% 10V CERM 402

PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM 87 mA (A01)
VOLTAGE=1.05V

MCP 3.3V/1.5V HDA Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

PP3V3_S0
7 mA (A01)

C2562 2.2UF 20% 6.3V CERM 402-LF

MCP79 Ethernet VRef

PP3V3_ENET

R2591 1.47K 1% 1/10W MF-LF 402
R2590 1.47K 1% 1/10W MF-LF 402
C2591 0.1UF 20% 10V CERM 402

MCP_MII_VREF (OUT)

L2588 30-OHM-1.7A 0402

C2588 4.7UF 20% 4V X5R 402
C2589 0.1UF 20% 10V CERM 402
C2590 0.1UF 20% 10V CERM 402

PP1V05_S0_MCP_PLL_NV
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM 37 mA (A01)
VOLTAGE=1.05V

PP1V05_ENET
5 mA (A01)

L2595 30-OHM-1.7A 0402

C2595 4.7UF 20% 4V X5R 402
C2596 0.1UF 20% 10V CERM 402

PP1V05_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM 5 mA (A01)
VOLTAGE=1.05V

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

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MCP Standard Decoupling

SYNC_MASTER=T18_MLB SYNC_DATE=02/05/2009

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE: NONE	SHT 22 OF 83	

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

66 53 17 7 6 PP1V8_S0
190 mA (A01, 1.8V)
C2610 2.2UF 20% 6.3V X5R CERM 402-LF

21 19 17 16 13 12 11 10 9 7 6 67 66 65 61 35 22 PP1V05_S0
95 mA (A01)
C2615 4.7UF 20% 6.3V X5R CERM 402
C2616 2.2UF 20% 6.3V X5R CERM 402-LF

77 17 MCP_HDMI_RSET
77 17 MCP_HDMI_VPROBE
NO STUFF
C2620 0.1UF 20% 16V CERM 402
R2620 1K 1% 1/16W MF-LF 402

77 17 MCP_IFPAB_RSET
77 17 MCP_IFPAB_VPROBE
NO STUFF
C2630 0.1UF 20% 16V CERM 402
R2630 1K 1% 1/16W MF-LF 402

NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)
PP3V3_S0_MCP_DAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
17
206 mA (A01)
R2651 0 5% 1/16W MF-LF 402

23 17 NC_MCP_RGB_RED — NC_MCP_RGB_RED 17 23
23 17 NC_MCP_RGB_GREEN — NC_MCP_RGB_GREEN 17 23
23 17 NC_MCP_RGB_BLUE — NC_MCP_RGB_BLUE 17 23
23 17 NC_MCP_RGB_HSYNC — NC_MCP_RGB_HSYNC 17 23
23 17 NC_MCP_RGB_VSYNC — NC_MCP_RGB_VSYNC 17 23
77 23 17 NC_CRT_IG_R_C_PR — NC_CRT_IG_R_C_PR 17 23 77
77 23 17 NC_CRT_IG_G_Y_Y — NC_CRT_IG_G_Y_Y 17 23 77
77 23 17 NC_CRT_IG_B_COMP_PB — NC_CRT_IG_B_COMP_PB 17 23 77
77 23 17 NC_CRT_IG_HSYNC — NC_CRT_IG_HSYNC 17 23 77
77 23 17 NC_CRT_IG_VSYNC — NC_CRT_IG_VSYNC 17 23 77
(MAKE_BASE=TRUE NO_TEST=TRUE)

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???

82 73 71 69 68 67 66 61 58 27 26 22 21 20 18 17 12 9 57 53 49 47 46 45 43 41 37 35 PP3V3_S0
16 mA (A01)
L2640 30-OHM-1.7A 0402
C2640 4.7UF 20% 6.3V CERM 603
C2641 0.1UF 20% 10V CERM 402
PP3V3_S0_MCP_VPLL
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
17
16 mA (A01)

23 17 NC_MCP_RGB_DAC_RSET — NC_MCP_RGB_DAC_RSET 17 23
23 17 NC_MCP_RGB_DAC_VREF — NC_MCP_RGB_DAC_VREF 17 23
77 23 17 NC_MCP_TV_DAC_RSET — NC_MCP_TV_DAC_RSET 17 23 77
77 23 17 NC_MCP_TV_DAC_VREF — NC_MCP_TV_DAC_VREF 17 23 77
23 17 NC_MCP_CLK27M_XTALIN — NC_MCP_CLK27M_XTALIN 17 23
23 17 NC_MCP_CLK27M_XTALOUT — NC_MCP_CLK27M_XTALOUT 17 23
(MAKE_BASE=TRUE NO_TEST=TRUE)

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MCP Graphics Support

SYNC_MASTER=K19_MLB SYNC_DATE=02/05/2009

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D	051-7903	A

SCALE: NONE SHT 23 OF 83

Current numbers from email Xiaowei Lin provided 11/12/2007 3:22pm (no official document number).

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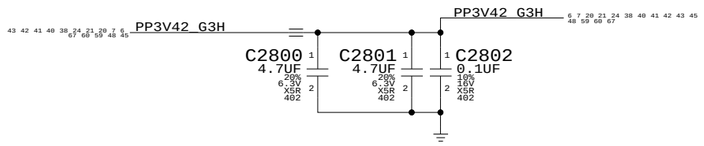
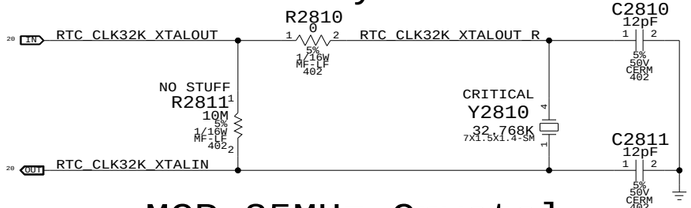
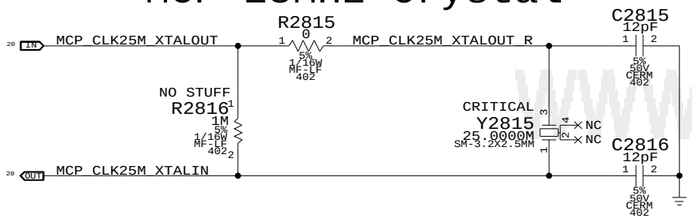
RTC Power Source



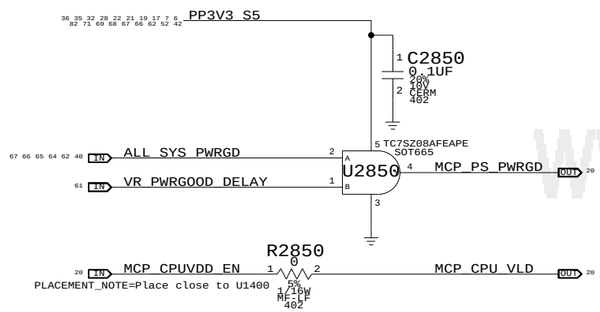
RTC Crystal



MCP 25MHz Crystal

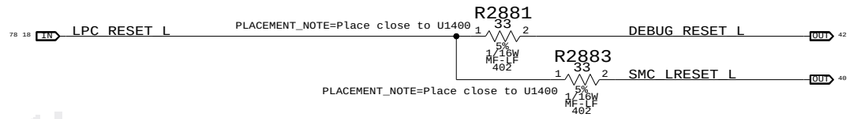


MCP S0 PWRGD & CPU_VLD

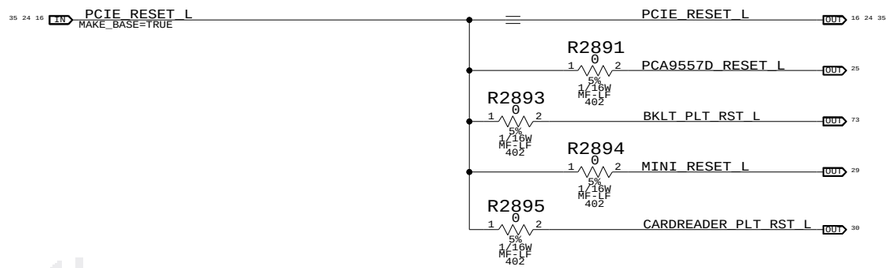


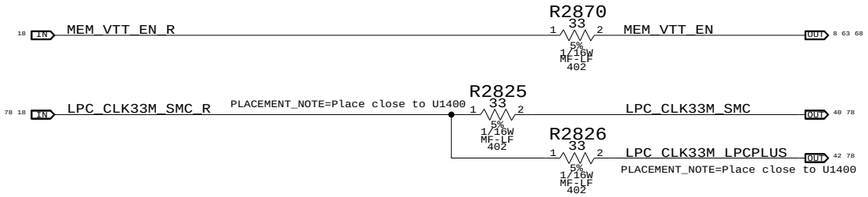
Platform Reset Connections

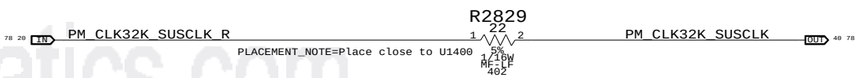
LPC Reset (Unbuffered)



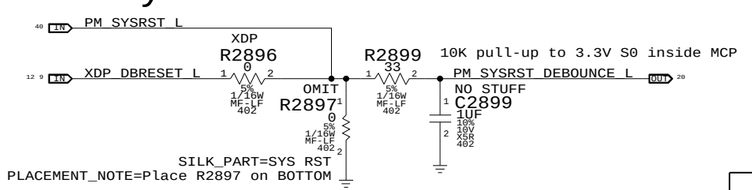
PCIE Reset (Unbuffered)







System Reset Circuit



SB Misc

SYNC_MASTER=WFERRY_K19I SYNC_DATE=01/06/2009

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A

SCALE	SHT	OF
NONE	24	83

Page Notes

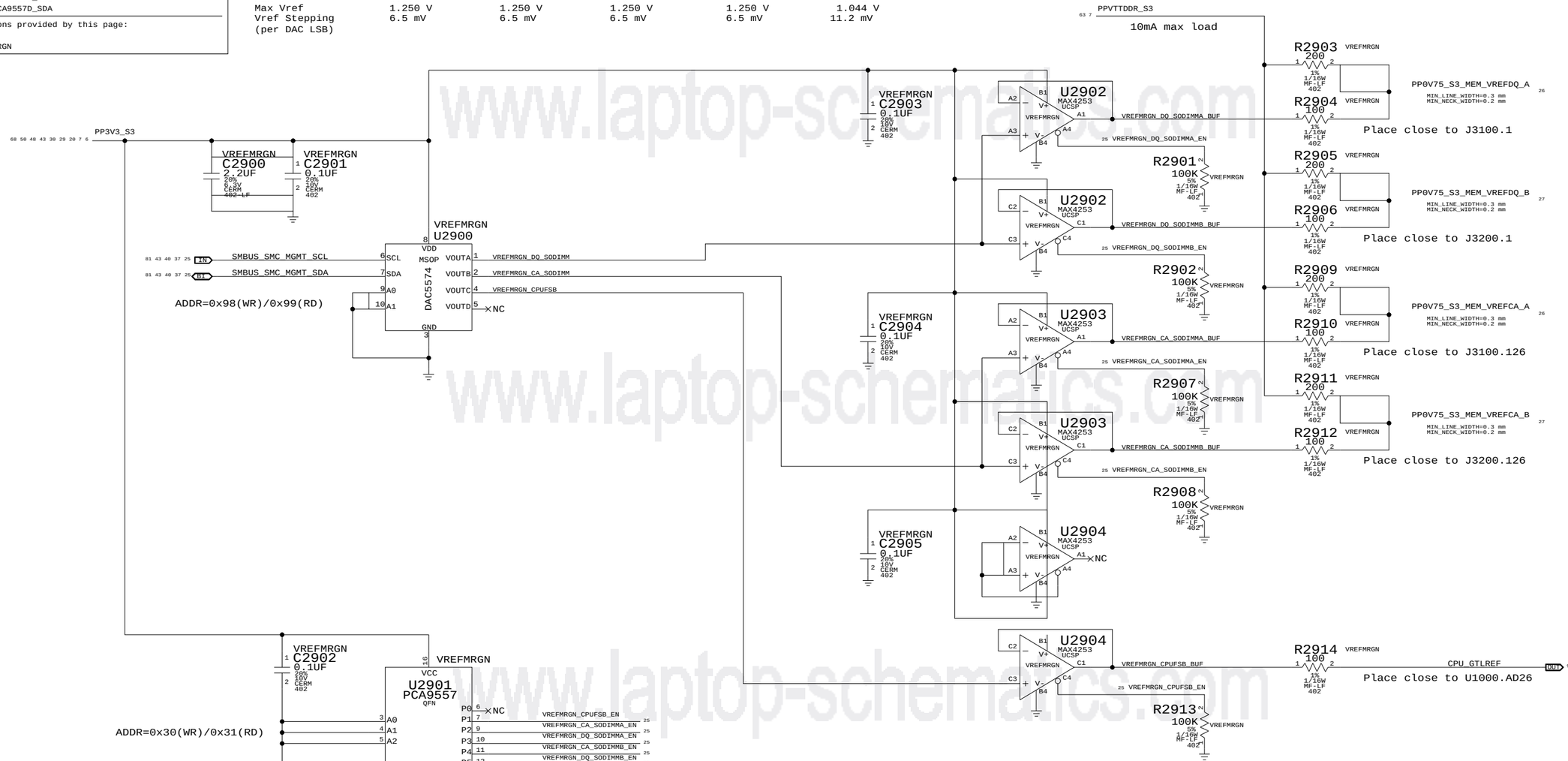
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3 Vref Margining

SYNC_MASTER=K24_MLB SYNC_DATE=02/05/2009

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE: NONE	SHT 25 OF 83	

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DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

GND

PP1V5_S3

C3100 10UF 20% 6.3V X6R 603
C3101 10UF 20% 6.3V X6R 603

C3110 C3111 C3112 C3113 C3114 C3115 C3116 C3117 C3118 C3119 C3120 C3121 C3122 C3123
0.1UF 20% 10V CERM 402

PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

PP0V75_S3_MEM_VREFCA_A

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

PP3V3_S0

C3140 2.2UF 20% 6.3V CERM 402-LF

R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

PP0V75_S0_DDRVTT

J3100 DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2) F-RT-THB

KEY

73	CKE0	CKE1	74
75	VDD	VDD	76
77	NC	A15	78
79	BA2	A14	80
81	VDD	VDD	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD	VDD	88
89	A8	A6	90
91	A5	A4	92
93	VDD	VDD	94
95	A3	A2	96
97	A1	A0	98
99	VDD	VDD	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD	VDD	106
107	A10/AP	BA1	108
109	BA0	RAS*	110
111	VDD	VDD	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD	VDD	118
119	A13	ODT1	120
121	S1*	NC	122
123	VDD	VDD	124
125	TEST	VREFCA	126
127	VSS	VSS	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS	VSS	134
135	DQS4*	DM4	136
137	DQS4	VSS	138
139	VSS	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS	144
145	VSS	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS	150
151	VSS	DQS5*	152
153	DM5	DQS5	154
155	VSS	VSS	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS	VSS	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS	VSS	168
169	DQS6*	DM6	170
171	DQS6	VSS	172
173	VSS	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS	178
179	VSS	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS	184
185	VSS	DQS7*	186
187	DM7	DQS7	188
189	VSS	VSS	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS	VSS	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT	VTT	204

516-0196

SPD ADDR=0xA0(WR)/0xA1(RD)

J3100 DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2) F-RT-THB

CRITICAL

KEY

1	VREFDQ	VSS	2
3	VSS	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS	8
9	VSS	DQS0*	10
11	DM0	DQS0	12
13	VSS	VSS	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS	VSS	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS	VSS	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS	VSS	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS	VSS	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS	VSS	44
45	DQS2*	DM2	46
47	DQS2	VSS	48
49	VSS	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS	54
55	VSS	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS	60
61	VSS	DQS3*	62
63	DM3	DQS3	64
65	VSS	VSS	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS	VSS	72

516-0196

"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=K19_MLB SYNC_DATE=02/05/2009

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D	051-7903	A
SCALE: NONE	SHT: 26 OF: 83	

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DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PP5FO_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

GND

68 63 28 26 7 6 PP1V5_S3

C3210 0.1UF 20% 10V CERM 402
C3211 0.1UF 20% 10V CERM 402
C3212 0.1UF 20% 10V CERM 402
C3213 0.1UF 20% 10V CERM 402
C3214 0.1UF 20% 10V CERM 402
C3215 0.1UF 20% 10V CERM 402
C3216 0.1UF 20% 10V CERM 402
C3217 0.1UF 20% 10V CERM 402
C3218 0.1UF 20% 10V CERM 402
C3219 0.1UF 20% 10V CERM 402
C3220 0.1UF 20% 10V CERM 402
C3221 0.1UF 20% 10V CERM 402
C3222 0.1UF 20% 10V CERM 402
C3223 0.1UF 20% 10V CERM 402

C3200 10UF 20% 6.3V X6S 603
C3201 10UF 20% 6.3V X6S 603

25 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 F-RT-BGA3 DDR3-SODIMM (2 OF 2)

76 14 IN	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	IN 14 76
		75	VDD	VDD	76		
		77	NC	A15	78	NC_MEM_B_A<15>	IN 8
76 14 IN	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>	IN 14 76
		81	VDD	VDD	82		
76 14 IN	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>	IN 14 76
76 14 IN	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>	IN 14 76
		87	VDD	VDD	88		
76 14 IN	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>	IN 14 76
76 14 IN	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>	IN 14 76
		93	VDD	VDD	94		
76 14 IN	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>	IN 14 76
76 14 IN	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>	IN 14 76
		99	VDD	VDD	100		
76 14 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	IN 14 76
76 14 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>	IN 14 76
		105	VDD	VDD	106		
76 14 IN	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>	IN 14 76
76 14 IN	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L	IN 14 76
		111	VDD	VDD	112		
76 14 IN	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>	IN 14 76
76 14 IN	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>	IN 14 76
		117	VDD	VDD	118		
76 14 IN	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>	IN 14 76
76 14 IN	MEM_B_CS_L<1>	121	S1*	NC	122		
		123	VDD	VDD	124		
		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
76 14 BI	MEM_B_DQ<32>	129	DQ32	DQ36	130	MEM_B_DQ<33>	BI 14 76
76 14 BI	MEM_B_DQ<37>	131	DQ33	DQ37	132	MEM_B_DQ<36>	BI 14 76
		133	VSS	VSS	134		
76 14 BI	MEM_B_DQS_N<4>	135	DQS4*	DM4	136	MEM_B_DM<4>	IN 14 76
76 14 BI	MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	MEM_B_DQ<38>	BI 14 76
76 14 BI	MEM_B_DQ<34>	141	DQ34	DQ39	142	MEM_B_DQ<39>	BI 14 76
76 14 BI	MEM_B_DQ<35>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	MEM_B_DQ<44>	BI 14 76
76 14 BI	MEM_B_DQ<41>	147	DQ40	DQ45	148	MEM_B_DQ<45>	BI 14 76
76 14 BI	MEM_B_DQ<40>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	MEM_B_DQS_N<5>	BI 14 76
76 14 IN	MEM_B_DM<5>	153	DM5	DQS5	154	MEM_B_DQS_P<5>	BI 14 76
		155	VSS	VSS	156		
76 14 BI	MEM_B_DQ<43>	157	DQ42	DQ46	158	MEM_B_DQ<47>	BI 14 76
76 14 BI	MEM_B_DQ<42>	159	DQ43	DQ47	160	MEM_B_DQ<46>	BI 14 76
		161	VSS	VSS	162		
76 14 BI	MEM_B_DQ<55>	163	DQ48	DQ52	164	MEM_B_DQ<48>	BI 14 76
76 14 BI	MEM_B_DQ<49>	165	DQ49	DQ53	166	MEM_B_DQ<54>	BI 14 76
		167	VSS	VSS	168		
76 14 BI	MEM_B_DQS_N<6>	169	DQS6*	DM6	170	MEM_B_DM<6>	IN 14 76
76 14 BI	MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	MEM_B_DQ<53>	BI 14 76
76 14 BI	MEM_B_DQ<52>	175	DQ50	DQ55	176	MEM_B_DQ<50>	BI 14 76
76 14 BI	MEM_B_DQ<51>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	MEM_B_DQ<60>	BI 14 76
76 14 BI	MEM_B_DQ<56>	181	DQ56	DQ61	182	MEM_B_DQ<61>	BI 14 76
76 14 BI	MEM_B_DQ<57>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	MEM_B_DQS_N<7>	BI 14 76
76 14 IN	MEM_B_DM<7>	187	DM7	DQS7	188	MEM_B_DQS_P<7>	BI 14 76
		189	VSS	VSS	190		
76 14 BI	MEM_B_DQ<63>	191	DQ58	DQ62	192	MEM_B_DQ<58>	BI 14 76
76 14 BI	MEM_B_DQ<59>	193	DQ59	DQ63	194	MEM_B_DQ<62>	BI 14 76
		195	VSS	VSS	196		
	MEM_B_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L	OUT 20 26 40
		199	VDDSPD	SDA	200	=I2C_SODIMMB_SDA	BI 43
	MEM_B_SA<1>	201	SA1	SCL	202	SMBUS_MCP_0_CLK	IN 12 20 26 43 78
		203	VTT	VTT	204	PP0V75_S0_DDRVTT	6 7 26 63 68
		205	MTG PIN	MTG PIN	206		
		207	MTG PIN	MTG PIN	208		
		209	MTG PIN	MTG PIN	210		
		211	MTG PIN	MTG PIN	212		

516s0704

SPD ADDR=0xA2(WR)/0xA3(RD)

R3240 10K 5% 1/16W MF-LF 402
R3241 10K 5% 1/16W MF-LF 402

61 58 57 53 49 47 21 20 14 12 9 6 62 72 71 69 68 67 66 46 45 PP3V3_S0

C3240 2.2UF 20% 6.3V CERM 402-LF

J3200 CRITICAL F-RT-BGA3 DDR3-SODIMM (1 OF 2)

		1	VREFDQ	VSS	2		
76 14 BI	MEM_B_DQ<0>	3	VSS	DQ4	4	MEM_B_DQ<4>	BI 14 76
76 14 BI	MEM_B_DQ<1>	5	DQ0	DQ5	6	MEM_B_DQ<5>	BI 14 76
		7	DQ1	VSS	8		
76 14 IN	MEM_B_DM<0>	9	VSS	DQS0*	10	MEM_B_DQS_N<0>	BI 14 76
		11	DM0	DQS0	12	MEM_B_DQS_P<0>	BI 14 76
		13	VSS	VSS	14		
76 14 BI	MEM_B_DQ<2>	15	DQ2	DQ6	16	MEM_B_DQ<6>	BI 14 76
76 14 BI	MEM_B_DQ<3>	17	DQ3	DQ7	18	MEM_B_DQ<7>	BI 14 76
		19	VSS	VSS	20		
76 14 BI	MEM_B_DQ<28>	21	DQ8	DQ12	22	MEM_B_DQ<29>	BI 14 76
76 14 BI	MEM_B_DQ<24>	23	DQ9	DQ13	24	MEM_B_DQ<25>	BI 14 76
		25	VSS	VSS	26		
76 14 BI	MEM_B_DQS_N<3>	27	DQS1*	DM1	28	MEM_B_DM<3>	IN 14 76
76 14 BI	MEM_B_DQS_P<3>	29	DQS1	RESET*	30	MEM_RESET_L	IN 26 28
		31	VSS	VSS	32		
76 14 BI	MEM_B_DQ<31>	33	DQ10	DQ14	34	MEM_B_DQ<26>	BI 14 76
76 14 BI	MEM_B_DQ<30>	35	DQ11	DQ15	36	MEM_B_DQ<27>	BI 14 76
		37	VSS	VSS	38		
76 14 BI	MEM_B_DQ<9>	39	DQ16	DQ20	40	MEM_B_DQ<13>	BI 14 76
76 14 BI	MEM_B_DQ<8>	41	DQ17	DQ21	42	MEM_B_DQ<12>	BI 14 76
		43	VSS	VSS	44		
76 14 BI	MEM_B_DQS_N<1>	45	DQS2*	DM2	46	MEM_B_DM<1>	IN 14 76
76 14 BI	MEM_B_DQS_P<1>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	MEM_B_DQ<14>	BI 14 76
76 14 BI	MEM_B_DQ<15>	51	DQ18	DQ23	52	MEM_B_DQ<11>	BI 14 76
76 14 BI	MEM_B_DQ<10>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	MEM_B_DQ<20>	BI 14 76
76 14 BI	MEM_B_DQ<21>	57	DQ24	DQ29	58	MEM_B_DQ<16>	BI 14 76
76 14 BI	MEM_B_DQ<17>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	MEM_B_DQS_N<2>	BI 14 76
76 14 IN	MEM_B_DM<2>	63	DM3	DQS3	64	MEM_B_DQS_P<2>	BI 14 76
		65	VSS	VSS	66		
76 14 BI	MEM_B_DQ<18>	67	DQ26	DQ30	68	MEM_B_DQ<19>	BI 14 76
76 14 BI	MEM_B_DQ<22>	69	DQ27	DQ31	70	MEM_B_DQ<23>	BI 14 76
		71	VSS	VSS	72		

516s0704

PP0V75_S3_MEM_VREFCA_B 25

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

SYNC_MASTER=K19_MLB SYNC_DATE=02/05/2009

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SCALE: NONE	SHT 27 OF 83	

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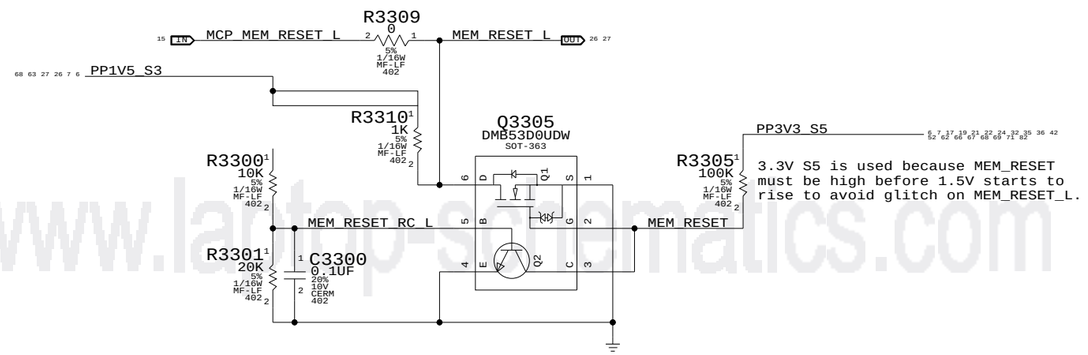
DDR3 RESET Support

Required becaues MCP79 does not meet DDR3 spec power-up reset timing requirement.



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DDR3 Support

SYNC_MASTER=T18_MLB SYNC_DATE=02/05/2009

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D	051-7903	A

SCALE	SHT	OF
NONE	28	83

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5V S3 WLAN FET

Part	TPCP8102
Type	P-Channel
Rds(on)	14 mOhm @4.5V
Loading	0.8 A (EDP)

PCIE_MINI_PRSNT_L
Q3401 SSM6N15FEAPE SOT563
AP_PWR_EN
MINI_CLKREQ_L
Q3401 SSM6N15FEAPE SOT563

1000 mA peak
750 mA nominal max

PLACEMENT_NOTE=Place close to J3401.
L3404 FERR-120-OHM-1.5A 0402-LF
PP5V_WLAN_F MIN_LINE_WIDTH=1 mm MIN_NECK_WIDTH=0.5 mm VOLTAGE=5V
C3421 0.1uF 10% 10V CERM 402
C3420 10UF 20% 10V X5R 0805
XW3450 SM
XW3451 SM
XW3452 SM
PP5V_WLAN_R MIN_LINE_WIDTH=1 mm MIN_NECK_WIDTH=0.5 mm VOLTAGE=5V

PLACEMENT_NOTES:
Place close to Q3450.
(C3420 & C3421)

CRITICAL
Q3450 TPCP8102 23V1K-SM
C3450 0.1UF 10% 16V X5R 402
C3451 0.033UF 10% 16V X5R 402
R3450 100K 5% 1/16W MF-LF 402
R3451 10K 5% 1/16W MF-LF 402
PP5V_S3
P5VWLAN_SS
PM_WLAN_EN_L

ISNS_AIRPORT_P
ISNS_AIRPORT_N

AIRPORT

CRITICAL
J3401 20347-325E-12 F-RT-SM

PCIE_MINI_D2R_P
PCIE_MINI_D2R_N
PCIE_MINI_R2D_P
PCIE_MINI_R2D_N
PCIE_CLK100M_MINI_CONN_P
PCIE_CLK100M_MINI_CONN_N
MINI_CLKREQ_Q_L
PCIE_WAKE_L
MINI_RESET_CONN_L
PP5V_WLAN
NC

C3431 0.1uF 10% 16V X5R 402 PLACEMENT_NOTE=Place close to J3401.
PCIE_MINI_R2D_C_P
C3430 0.1uF 10% 16V X5R 402 PLACEMENT_NOTE=Place close to J3401.
PCIE_MINI_R2D_C_N

CRITICAL
L3401 90-OHM-100MA DLP11S SYM_VER-1
PCIE_CLK100M_MINI_P
PCIE_CLK100M_MINI_N
PLACEMENT_NOTE=Place close to J3401.

MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

PP3V3_S3
U3402 74LVC1G17DRL SOT-553
TC7SZ08AFEAPE SOT665
U3401
WLAN_SMIT_BUF
WLAN_SMIT_RC
R3453 33K 5% 1/10W MF-LF 402
R3455 1 5% 1/10W MF-LF 402
R3454 62K 5% 1/10W MF-LF 402
C3453 1UF 10% 6.3V CERM 402
WLAN_SMIT_DISCHRG
Q3455 SSM3K15FV SOD-VESM-HF
MINI_RESET_L

PP3V3_S3_BT_F MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=3.3V
L3406 FERR-120-OHM-1.5A 0402-LF
PP3V3_S3
C3462 0.1uF 20% 10V CERM 402

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

275 mA peak
206 mA nominal max

PLACEMENT_NOTE=Place close to J3401.
L3405 FERR-120-OHM-1.5A 0402-LF
PP5V_S3
C3452 0.1uF 20% 10V CERM 402

ALS CAMERA

CRITICAL
L3402 90-OHM DLP0NS SYM_VER-1
USB_CAMERA_P
USB_CAMERA_N
PLACEMENT_NOTE=Place close to J3401.

PP5V_S3_BTCAMERA_F
SMBUS_SMC_A_S3_SDA
SMBUS_SMC_A_S3_SCL
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N
CONN_USB2_BT_P
CONN_USB2_BT_N
C3422 0.1uF 20% 10V CERM 402
518S0610

BLUETOOTH

CRITICAL
L3403 90-OHM DLP0NS SYM_VER-1
USB_BT_P
USB_BT_N
PLACEMENT_NOTE=Place close to J3401.

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Right Clutch Connector

SYNC_MASTER=K19_MLB SYNC_DATE=03/04/2009

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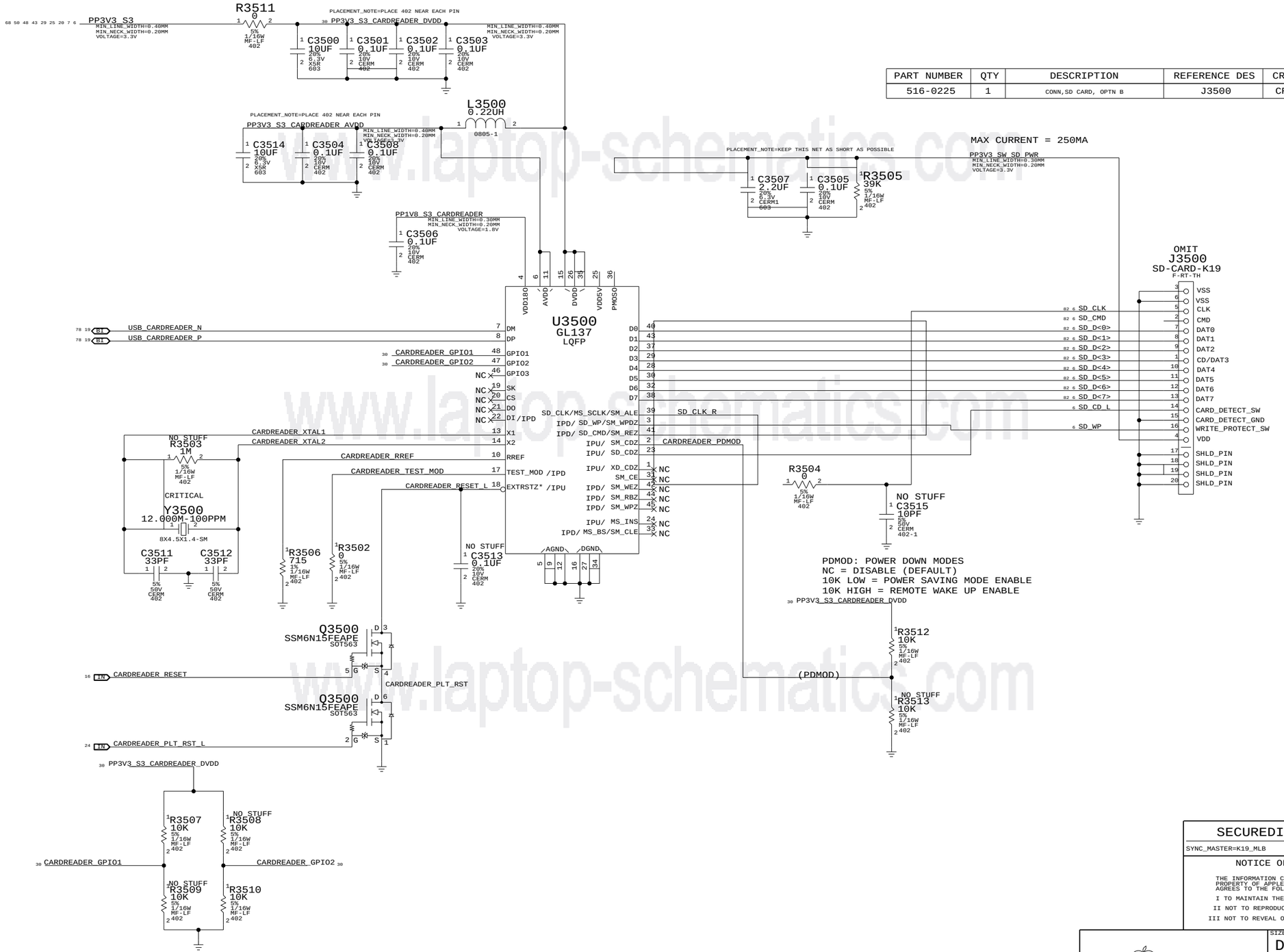
SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE: NONE	SHT 29 OF 83	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
516-0225	1	CONN,SD CARD, OPTN B	J3500	CRITICAL	



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SECUREDIGITAL CARD READER

SYNC_MASTER=K19_MLB SYNC_DATE=03/23/2009

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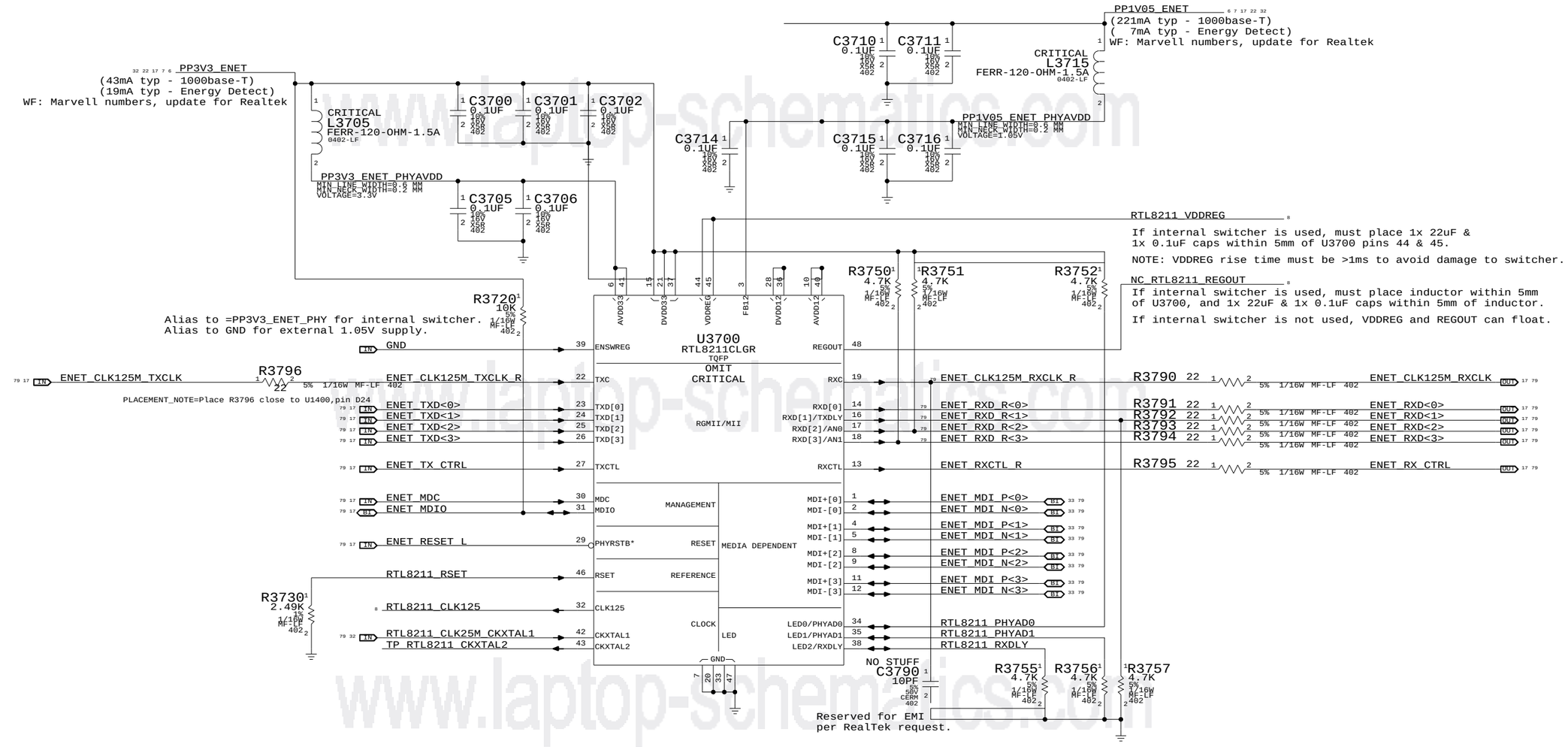
SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE: NONE	SHT 30 OF 83	



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Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

SYNC_MASTER=(K19I_MLB) SYNC_DATE=02/05/2009

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SCALE: NONE	SHT 31 OF 83	

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3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

CRITICAL
Q3810
NTR4101P
SOT-23-HF

35 32 28 24 22 21 19 17 7 6
82 71 69 68 67 66 62 52 42 36 PP3V3_S5

R3800 10K 5% 1/16W MF-LF 402

C3811 0.033UF 10% 16V X5R 402

PP3V3_ENET 6 7 17 22 31

R3810 100K 5% 1/16W MF-LF 402

P3V3ENET_EN_L

P3V3ENET_SS

C3810 0.01UF 10% 16V CERM 402

Q3801 SSM6N15FEAPE SOT563

32 20 8 IN PM_SLP_RMGT_L

MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

PM_WLAN_EN_L OUT 29

Pull-up is with power FET.

Q3805 SSM6N15FEAPE SOT563

29 20 IN AP_PWR_EN

AC_OR_S0_L

Q3805 SSM6N15FEAPE SOT563

Q3801 SSM6N15FEAPE SOT563

41 40 35 20 IN SMC_ADAPTER_EN

71 67 40 35 20 6 IN PM_SLP_S3_L

1.05V ENET FET

66 22 21 7 6 PP1V05_S5

C3840 0.1UF 10% 16V CERM 402

1.8V Vgs

CRITICAL

Q3840 SI2312BDS SOT23

35 32 28 24 22 21 19 17 7 6
82 71 69 68 67 66 62 52 42 36 PP3V3_S5

R3840 100K 5% 1/16W MF-LF 402

P1V05ENET_SS

PP1V05_ENET 6 7 17 22 31

R3842 69.8K 1% 1/16W MF-LF 402

Q3841 SSM6N15FEAPE SOT563

R3841 10K 1% 1/16W MF-LF 402

P1V05ENET_EN_L

C3841 0.01UF 10% 16V CERM 402

P1V05ENET_EN_L_RC

Q3841 SSM6N15FEAPE SOT563

32 20 8 IN PM_SLP_RMGT_L

Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

79 17 IN MCP_CLK25M_BUF0_R

R3895 22 5% 1/16W MF-LF 402

RTL8211_CLK25M_CKXTAL1 OUT 31 79

PLACEMENT_NOTE=Place close to U1400

Ethernet & AirPort Support

SYNC_MASTER=K19_MLB SYNC_DATE=02/05/2009

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D	051-7903	A

SCALE	SHT	OF
NONE	32	83

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

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Place one of 0.1uf cap close to each centertap pin of transformer

ENETCONN_CTAP

C3900 0.1UF 10% 16V X5S 402
C3902 0.1UF 10% 16V X5S 402
C3904 0.1UF 10% 16V X5S 402
C3906 0.1UF 10% 16V X5S 402

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_N<1>
ENET_MDI_P<1>
ENET_MDI_N<2>
ENET_MDI_P<2>
ENET_MDI_N<3>
ENET_MDI_P<3>

CRITICAL
T3900
SM
TX
TLA-6T213HF
RX

1 ENETCONN_P<0>
2 ENETCONN_N<0>
3 ENET_CTAP0
4 ENET_CTAP1
5 ENETCONN_N<1>
6 ENETCONN_P<1>

CRITICAL
T3901
SM
TX
TLA-6T213HF
RX

1 ENETCONN_N<2>
2 ENETCONN_P<2>
3 ENET_CTAP2
4 ENET_CTAP3
5 ENETCONN_N<3>
6 ENETCONN_P<3>

CRITICAL
J3900
RJ45-M97-3
F-RT-TH
514-0636

Transformers should be mirrored on opposite sides of the board

R3900 75 1/16W 5% MF-LF 402
R3901 75 1/16W 5% MF-LF 402
R3902 75 1/16W 5% MF-LF 2402
R3903 75 1/16W 5% MF-LF 2402

CRITICAL
C3908
1000PF
10%
2KV
CERM
1206

ENET_BOB_SMITH_CAP
MIN_LINE_WIDTH=0.9 mm
MIN_NECK_WIDTH=0.25 mm

CRITICAL
C3910 10PF 5% 50V CERM 402-1
C3911 10PF 5% 50V CERM 402-1
C3920 10PF 5% 50V CERM 402-1
C3921 10PF 5% 50V CERM 402-1
C3930 10PF 5% 50V CERM 402-1
C3931 10PF 5% 50V CERM 402-1
C3940 10PF 5% 50V CERM 402-1
C3941 10PF 5% 50V CERM 402-1

PLACEMENT_NOTE=Place on MDI lines so there are no stubs all 8 caps.

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Ethernet Connector

SYNC_MASTER=K19_MLB SYNC_DATE=03/13/2009

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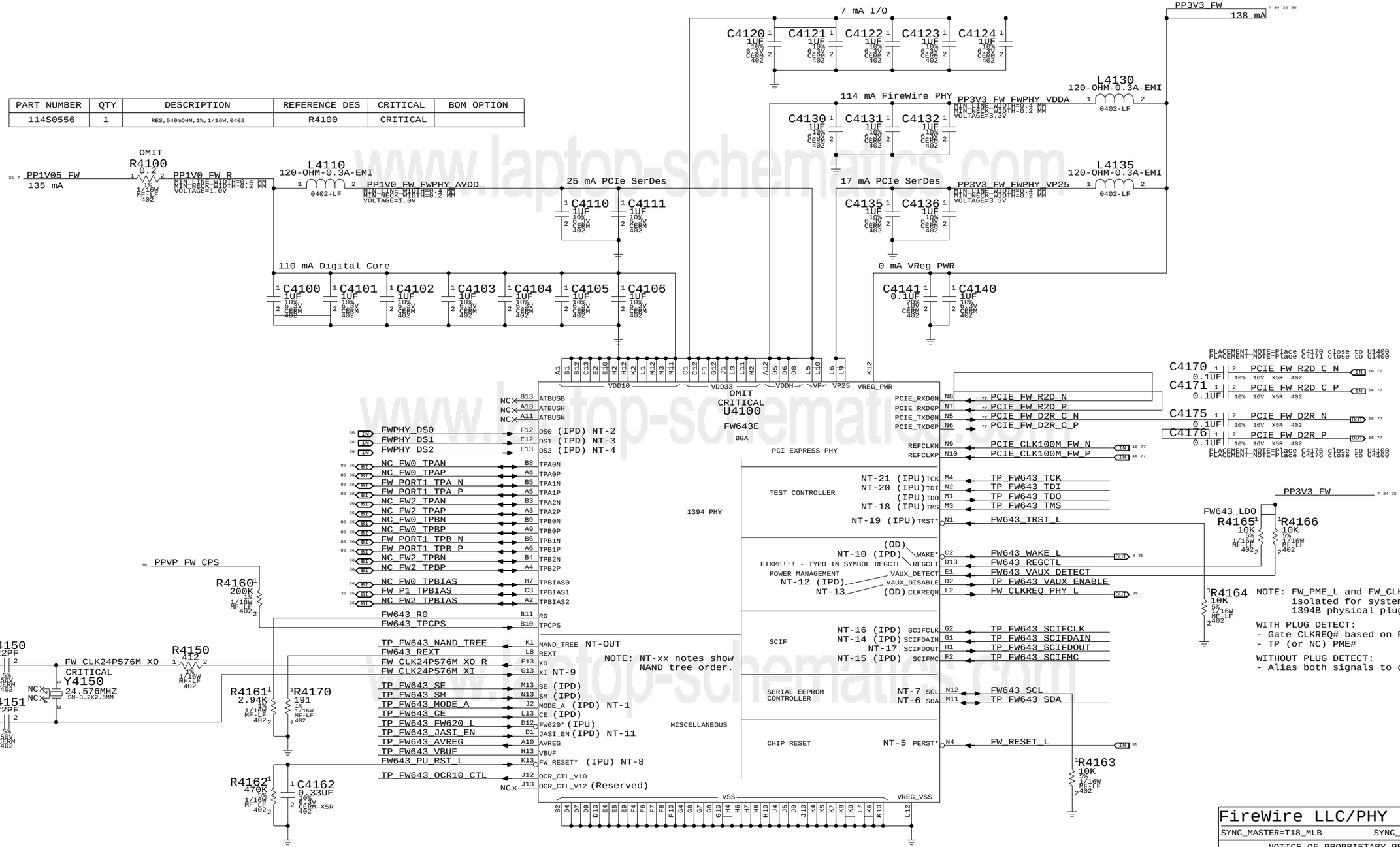
D	051-7903	A

SCALE	SHT	OF
NONE	33	83

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0556	1	RES,549mOHM,1%,1/16W,0402	R4100	CRITICAL	



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FireWire LLC/PHY (FW643E)

SYNC_MASTER=T18_MLB SYNC_DATE=02/05/2009

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE: NONE	SHT 34 OF 83	

Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

3.3V FW FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

PP3V3_S0
R4290 10K 5% 1/16W MF-LF 402
CRITICAL Q4291 NTR4101P SOT-23-HF
PP3V3_FW
C4290 0.033UF 10% 16V X5R 402
C4291 0.01UF 10% 16V CERM 402
P3V3FW_EN_L
R4291 100K 5% 1/16W MF-LF 402
P3V3FW_SS
Q4290 SSM6N15FEAPE SOT563
FW_PWR_EN

1.05V FW FET

PP1V05_S0
C4296 0.1UF 20% 16V CERM 402
PP3V3_FW
R4297 220K 5% 1/16W MF-LF 402
CRITICAL Q4295 SI2312BDS SOT23
P1V05FW_SS
Q4293 SSM6N15FEAPE SOT563
PP1V05_FW
NOSTUFF C4295 0.068UF 10% 16V CERM 402
R4295 10K 5% 1/16W MF-LF 402
P1V05_FW_EN_L
R4296 100K 5% 1/16W MF-LF 402
P1V05_FW_EN_L_RC
Q4293 SSM6N15FEAPE SOT563
FW_PWR_EN

PP3V3_FW
R4277 10K 5% 1/16W MF-LF 402
R4276 100K 5% 1/16W MF-LF 402
FW_PLUG_DET_L
FW_WAKE
NOSTUFF C4276 0.1UF 10% 16V X5R 402
CRITICAL Q4276 DMB53D0UV SOT-563
FW643_WAKE_L
CRITICAL Q4276 DMB53D0UV SOT-563
PP3V3_S5

PCIE_FW_PRSNT_L
MAKE_BASE=TRUE
Q4264 SSM6N15FEAPE SOT563
FW_CLKREQ_L
Q4264 SSM6N15FEAPE SOT563
FW_PWR_EN
FW_CLKREQ_PHY_L
MAKE_BASE=TRUE

PP3V3_S0
R4281 100K 5% 1/16W MF-LF 402
R4280 10K 1% 1/16W MF-LF 402
PP1V05_FW
CRITICAL Q4299 DMB53D0UV SOT-563
C4281 1UF 10% 6.3V CERM 402
P1V0_FW_RC
P1V0_RESET_GATE
R4283 10K 5% 1/16W MF-LF 402
PCIE_RESET_L
CRITICAL Q4299 DMB53D0UV SOT-563
FW_RESET_L
PP1V05_FW PGOOD/FW_RESET_L

FireWire Port Power Switch

PPBUS_G3H
CRITICAL Q4260 NDS9407 SOI-HF
PPBUS_FW_FWPWRSW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
CRITICAL F4260 1.1A-24V MINISMDC110H24
PPBUS_FW_FWPWRSW_D
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
CRITICAL D4260 SM CRS08-1.5A-30V
PPVP_FW

Late-VG Event Detection

CRITICAL Q4262 DMB54D0UV SOT-563
R4265 10K 5% 1/16W MF-LF 402
LATEVG_FAULT_EVENT_PNP
LATEVG_FAULT_EVENT
NOSTUFF R4263 100 1% 1/16W MF-LF 402
LATEVG_RETRY_RC
NOSTUFF C4263 1UF 10% 10V X5R 402-1

R4260 470K 5% 1/16W MF-LF 402
C4260 0.1UF 20% 25V X5R 402
FWPWR_EN_L_DIV
R4261 330K 5% 1/16W MF-LF 402
PP1V05_S0
FWPWR_EN_L
Q4261 SSM6N15FEAPE SOT563
Q4261 SSM6N15FEAPE SOT563
SMC_ADAPTER_EN
PM_SLP_S3_L
Enables port power when machine is running or on AC.

R4275 1K 5% 1/16W MF-LF 402
R4270 330K 5% 1/16W MF-LF 402
R4271 56K 5% 1/16W MF-LF 402
PP3V3_S0
R4274 100K 5% 1/16W MF-LF 402
FW_PLUG_DET_L
FW_DET_MIRROR
FW_PLUG_DET
CRITICAL Q4270 BC847CDXV6TXG SOT563
CRITICAL Q4270 BC847CDXV6TXG SOT563
C4270 0.1UF 10% 16V X5R 402
CRITICAL Q4275 DMB53D0UV SOT-563
FW_PWR_EN_L
FW_P1_TPBIAS_R
FW_DET_EMIT
R4272 1K 5% 1/16W MF-LF 402
R4273 12K 5% 1/16W MF-LF 402
CRITICAL Q4275 DMB53D0UV SOT-563
FW_PWR_EN
FW_P1_TPBIAS

PP3V3_S5
PP2V4_FW_LATEVG
R4211 10K 5% 1/16W MF-LF 402
R4212 10K 1% 1/16W MF-LF 402
C4210 0.1UF 10% 16V CERM 402
FWLATEGV_3V_REF
U4210 LMC7211 SM-HF
P2V4_FWLATEVG_RC
LATEVG_EVENT
C4211 100PF 5% 50V CERM 402
R4213 80.6K 1% 1/16W MF-LF 402
R4210 200K 1% 1/16W MF-LF 402

FWLATEVG Hysteresis:
3.08V when port power is on
2.91V when late Vg event and port power is off

FireWire Port Power

SYNC_MASTER=K19_MLB
SYNC_DATE=03/18/2009

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APPLE INC.
SIZE D | DRAWING NUMBER 051-7903 | REV. A
SCALE NONE | SHT 35 OF 83

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Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

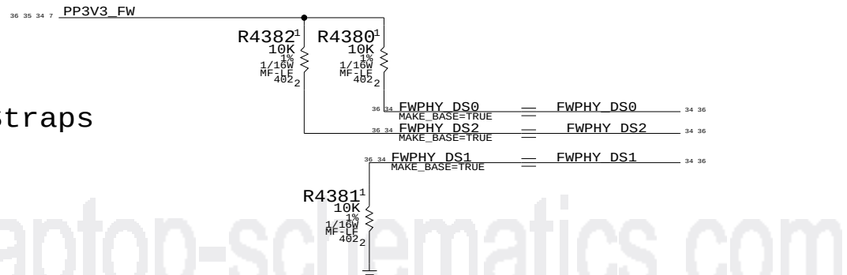
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

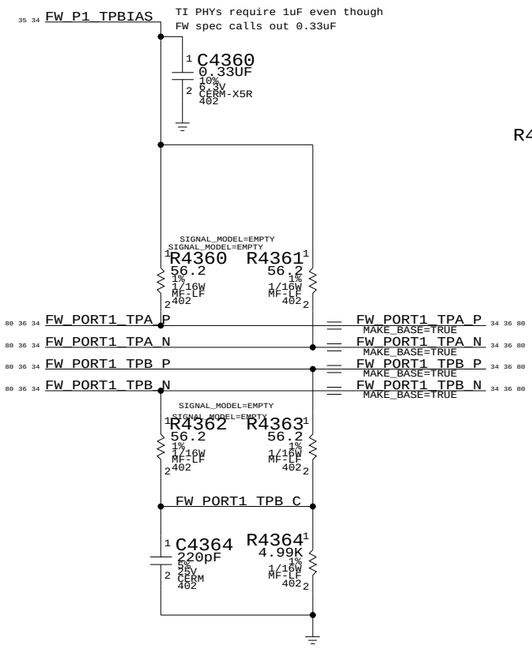
- 1-port Portable Power Class (0)

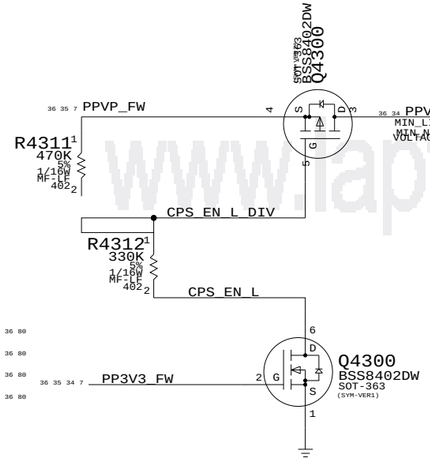
- Port "1" Bilingual (1394B)

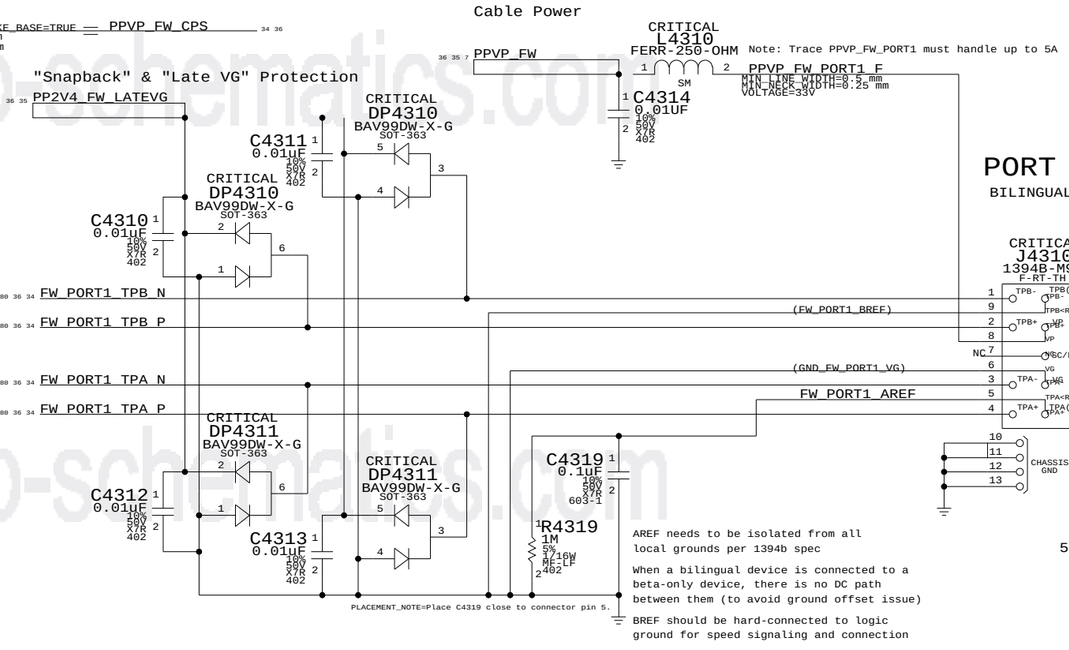


Termination

Place close to FireWire PHY





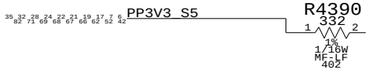


AREF needs to be isolated from all local grounds per 1394b spec

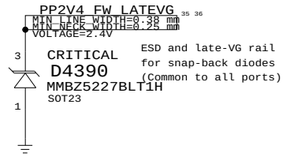
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

Late-VG Protection Power



PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail



ESD and late-VG rail for snap-back diodes (Common to all ports)

FireWire Ports

SYNC_MASTER=K19_MLB SYNC_DATE=02/05/2009

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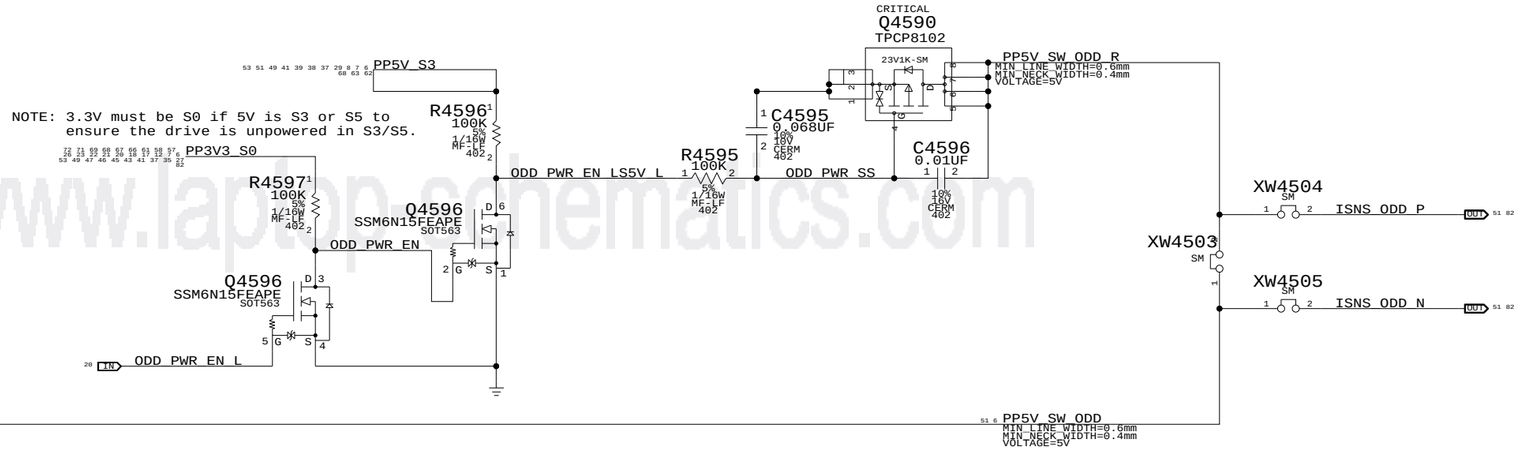
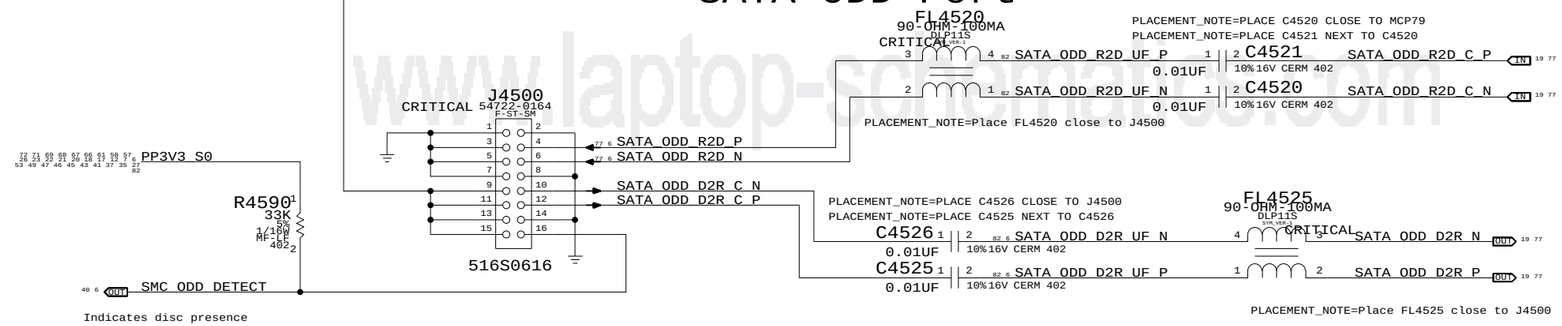
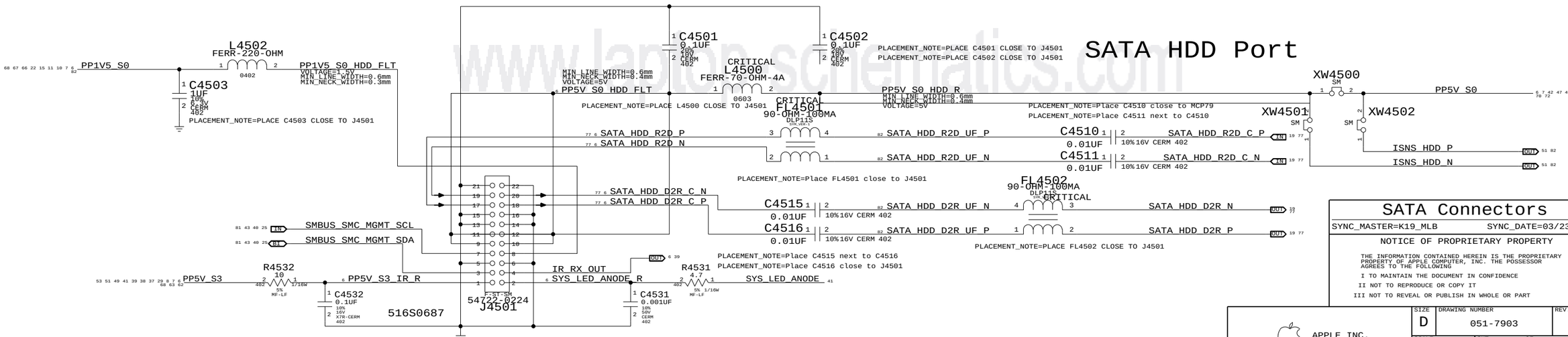
ODD Power Control



SATA ODD Port



SATA HDD Port



SATA Connectors

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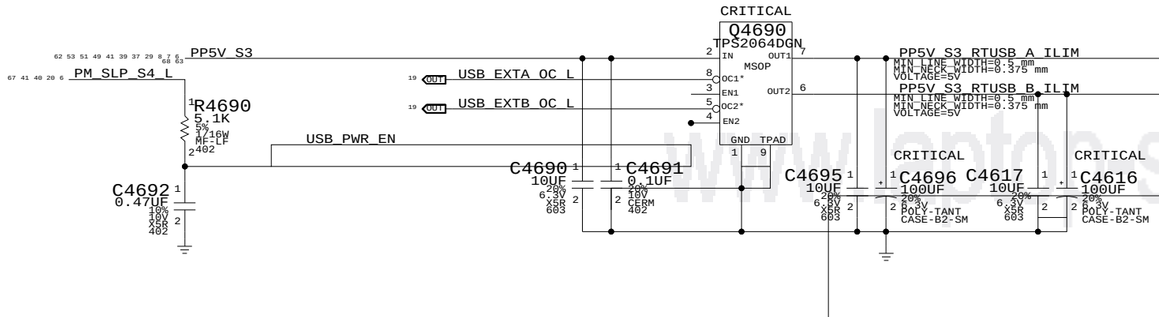
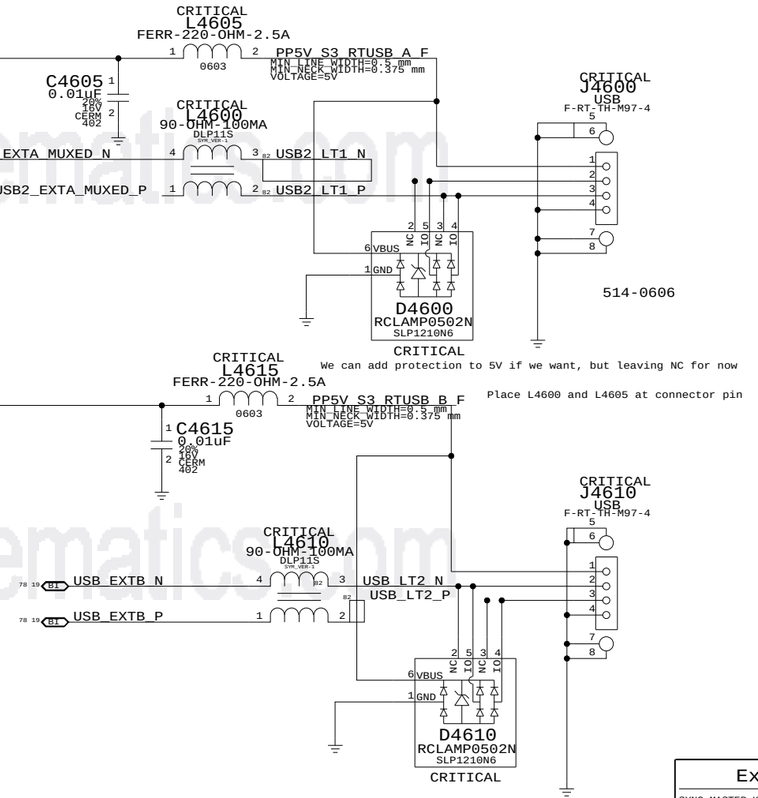
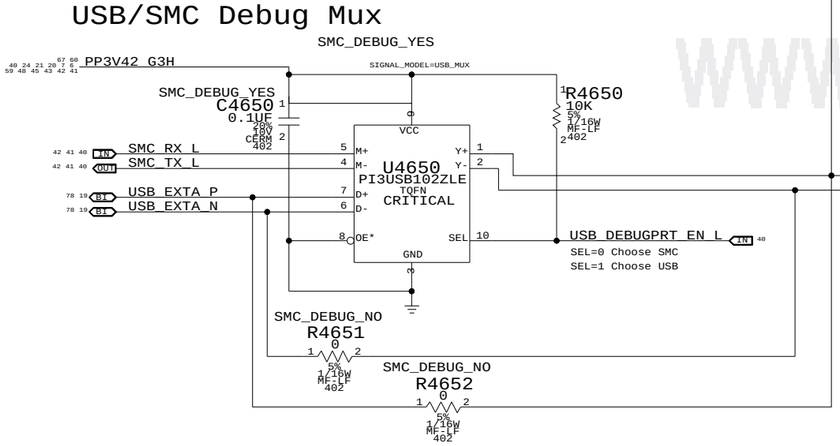
Port Power Switch



Left USB Port A



USB/SMC Debug Mux



Left USB Port B

External USB Connectors		
SYNC_MASTER=K19_MLB	SYNC_DATE=02/05/2009	

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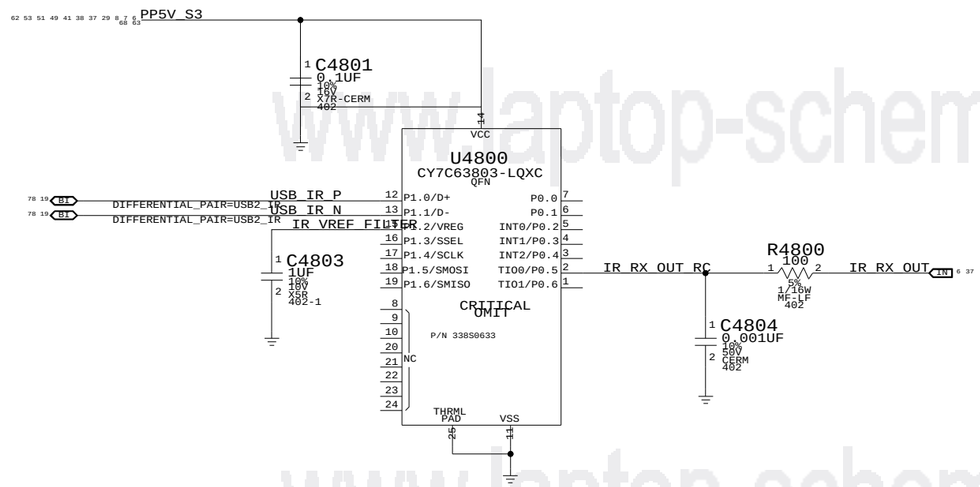
IR SUPPORT



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Front Flex Support

SYNC_MASTER=K19_MLB SYNC_DATE=02/05/2009

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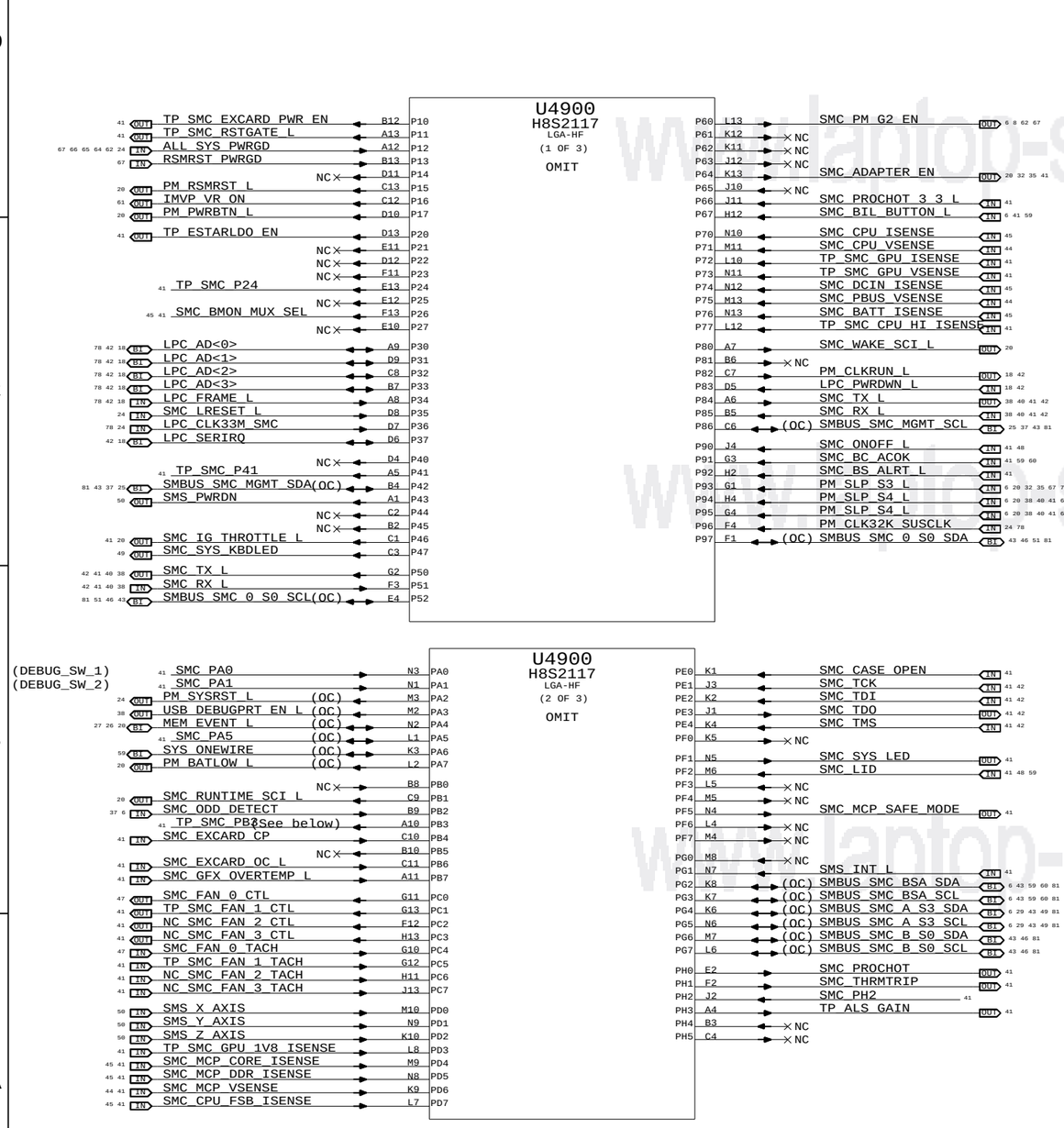
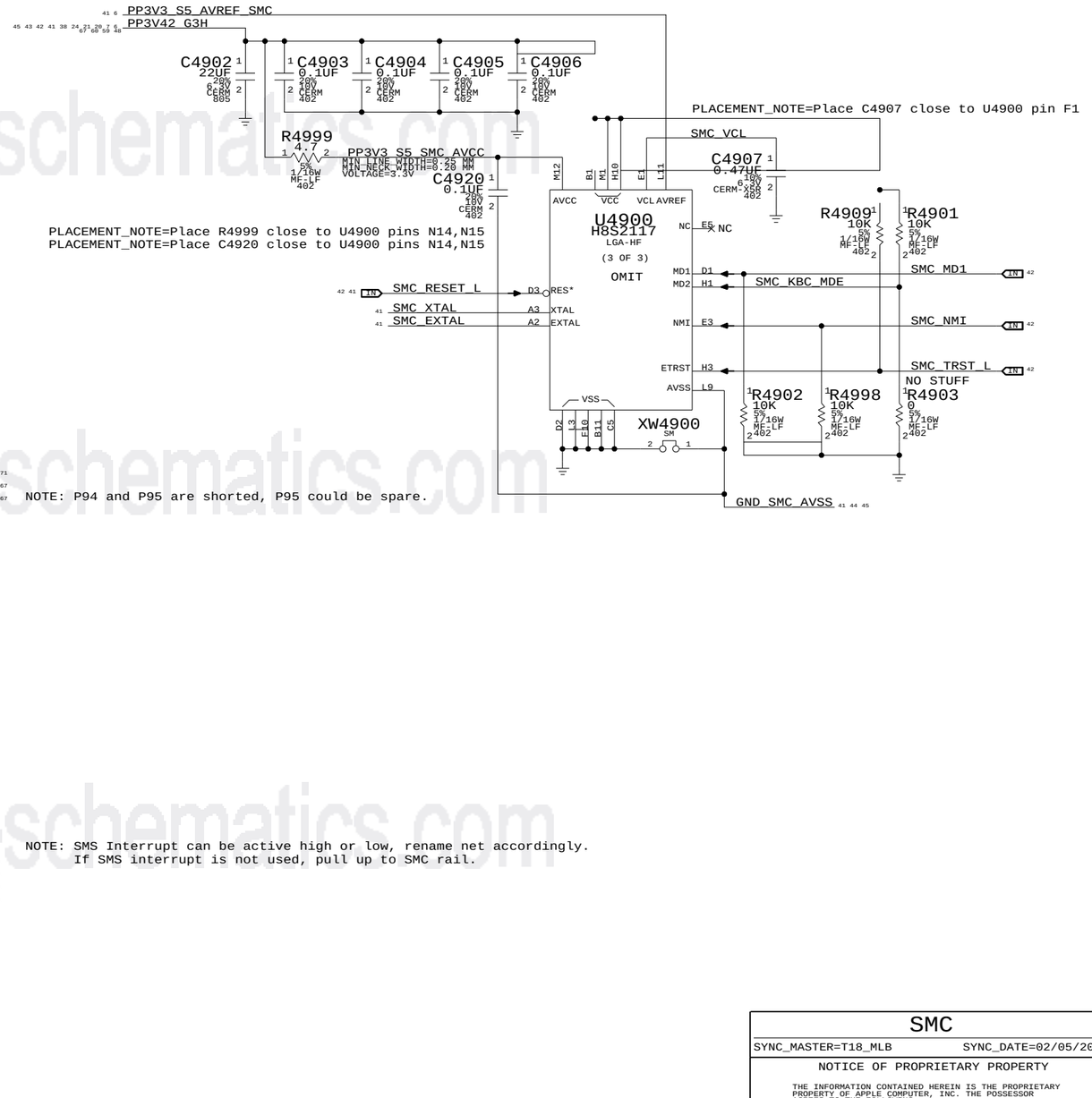
D	051-7903	A
SCALE	SHT	OF
NONE	39	83

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designed as inputs require pull-ups.



SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

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SMC

SYNC_MASTER=T18_MLB SYNC_DATE=02/05/2009

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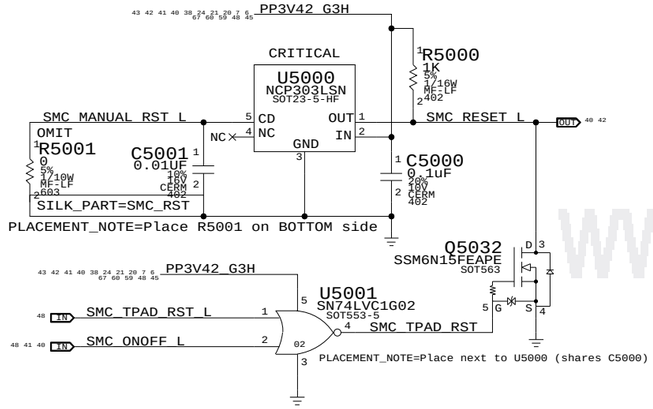
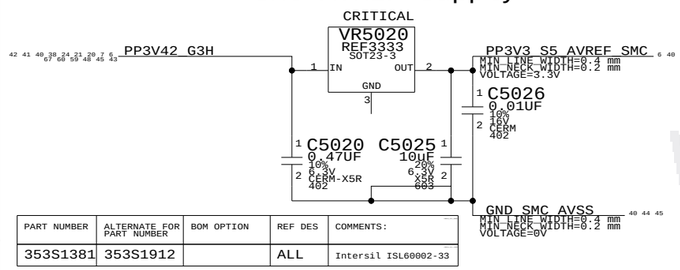
SCALE: NONE	SHT 40 OF 83	

SMC Reset "Button" / Brownout Detect

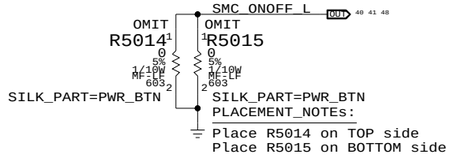


SMC AVREF Supply

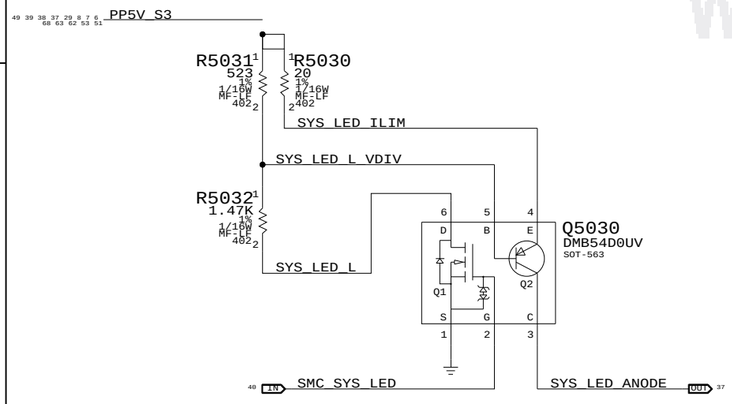


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

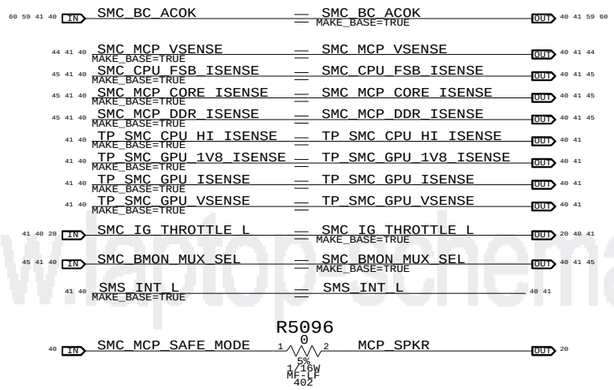
Debug Power "Buttons"



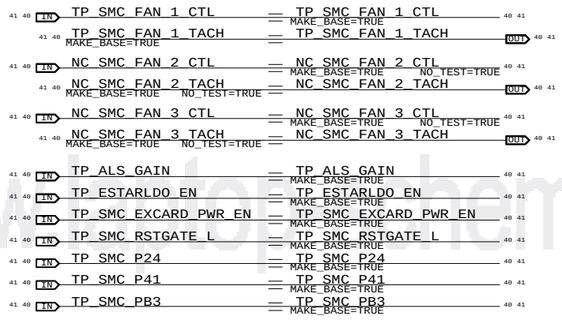
System (Sleep) LED Circuit



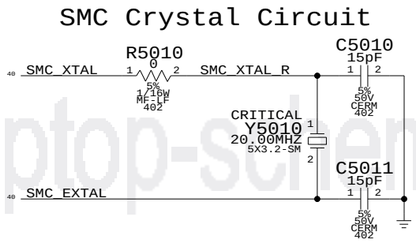
SMC Aliases



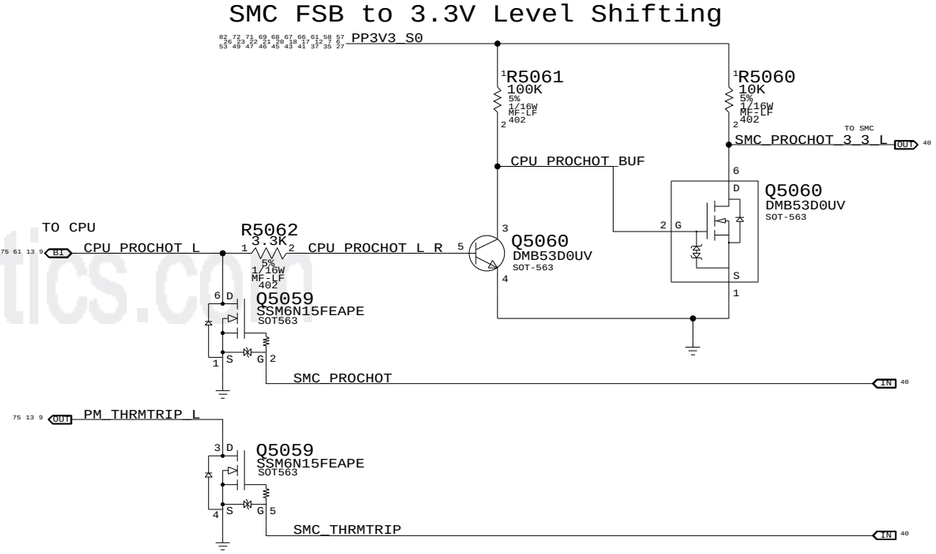
Unused Pins



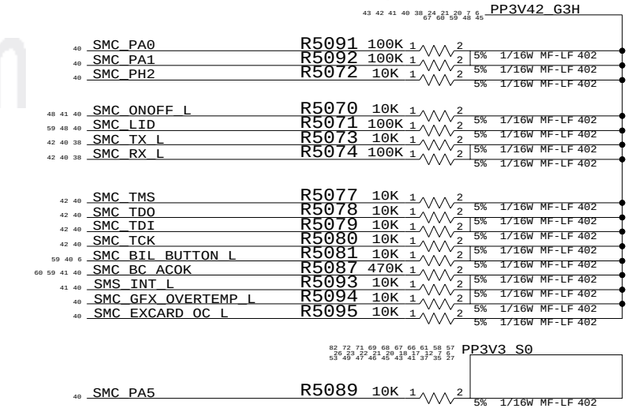
SMC Crystal Circuit



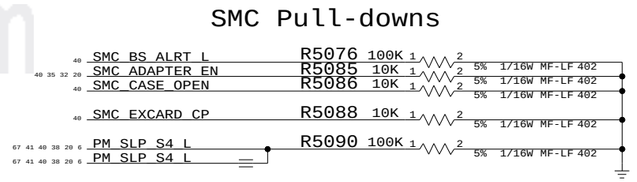
SMC FSB to 3.3V Level Shifting



SMC Pull-ups



SMC Pull-downs



SMC Support

SYNC_MASTER=(K19_MLB) SYNC_DATE=(11/25/2008)

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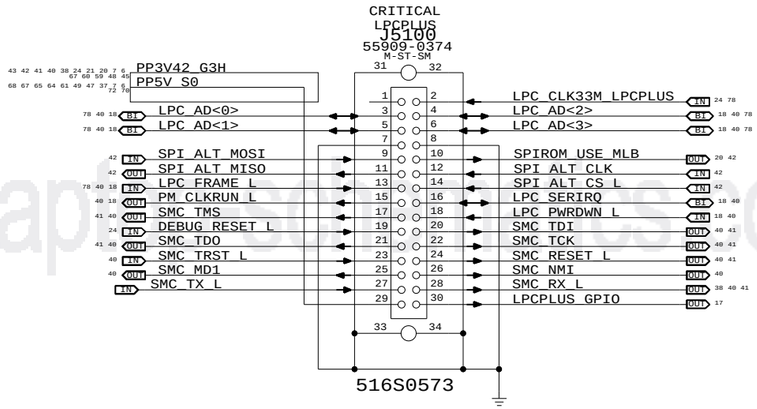
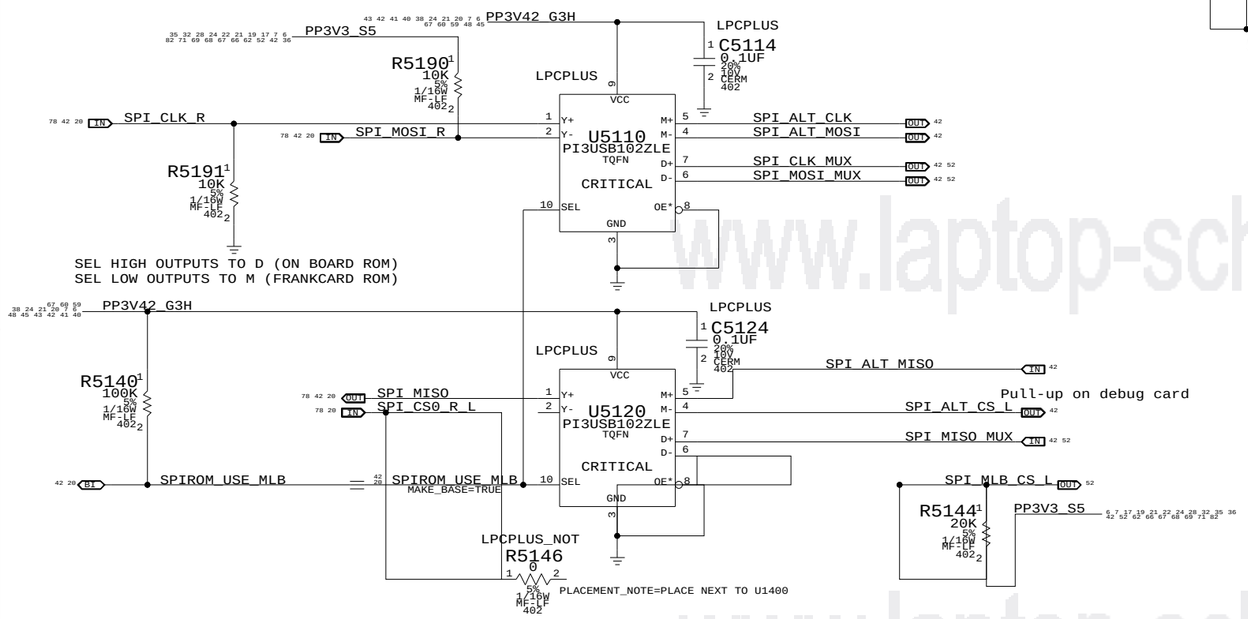
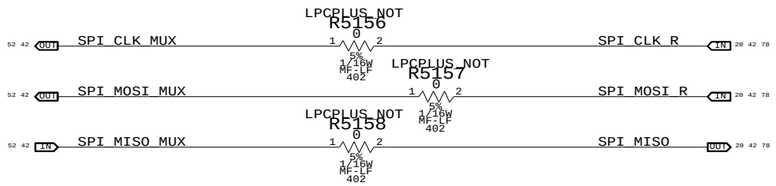
LPC+SPI Connector



Alternate SPI ROM Support



SPI MUX BYPASS



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LPC+SPI Debug Connector

SYNC_MASTER=K19_MLB SYNC_DATE=02/05/2009

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SCALE: NONE	SHT 42 OF 83	

MCP79 SMBUS "0" CONNECTIONS

PP3V3_S0

MCP79
U1400
(MASTER)

SMBUS_MCP_0_CLK (MAKE_BASE=TRUE)
SMBUS_MCP_0_DATA (MAKE_BASE=TRUE)

R5200 1K 5% 1/16W MF-LF 402
R5201 1K 5% 1/16W MF-LF 402

SO-DIMM "A"
J3100
(Write: 0xA0 Read: 0xA1)

SMBUS_MCP_0_CLK
SMBUS_MCP_0_DATA

SO-DIMM "B"
J3200
(Write: 0xA2 Read: 0xA3)

SMBUS_MCP_0_CLK
=I2C_SODIMMB_SDA

SMC "0" SMBus Connections

PP3V3_S0

SMC
U4900
(MASTER)

SMBUS_SMC_0_S0_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_0_S0_SDA (MAKE_BASE=TRUE)

R5250 4.7K 5% 1/16W MF-LF 402
R5251 4.7K 5% 1/16W MF-LF 402

MCP Temp
EMC1403-5: U5535
(Write: 0x98 Read: 0x99)

SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA

Sensor ADCs
U5930
(Write: 0x10 Read: 0x11)

SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

PP3V3_S3

SMC
U4900
(MASTER)

SMBUS_SMC_A_S3_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_A_S3_SDA (MAKE_BASE=TRUE)

R5270 1K 5% 1/16W MF-LF 402
R5271 1K 5% 1/16W MF-LF 402

TRACKPAD
J5800
(Write: 0x90 Read: 0x91)

SMBUS_SMC_A_S3_SCL
SMBUS_SMC_A_S3_SDA

ALS
J3401
(Write: 0x52 Read: 0x53)

SMBUS_SMC_A_S3_SCL
SMBUS_SMC_A_S3_SDA

MCP79 SMBUS "1" CONNECTIONS

PP3V3_S0

MCP79
U1400
(MASTER/SLAVE)

SMBUS_MCP_1_CLK (MAKE_BASE=TRUE)
SMBUS_MCP_1_DATA (MAKE_BASE=TRUE)

R5230 2.0K 5% 1/16W MF-LF 402
R5231 2.0K 5% 1/16W MF-LF 402

Mikey
U6860
(WRITE: 0X72 READ: 0X73)

SMBUS_MCP_1_CLK
SMBUS_MCP_1_DATA

LP8543 (Bklt)
U9700 (DEFAULT)
(Write: 0x58 Read: 0x59)

SMBUS_MCP_1_CLK
SMBUS_MCP_1_DATA

SMC "Battery A" SMBus Connections

PP3V42_G3H

SMC
U4900
(MASTER)

SMBUS_SMC_BSA_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_BSA_SDA (MAKE_BASE=TRUE)

R5280 2.61K 1% 1/16W MF-LF 402
R5281 2.61K 1% 1/16W MF-LF 402

BATTERY & BIL
J6950 & J6955
(See Table)

SMBUS_SMC_BSA_SCL
SMBUS_SMC_BSA_SDA

Battery Charger
ISL6258A - U7000
(Write: 0x12 Read: 0x13)

SMBUS_SMC_BSA_SCL
SMBUS_SMC_BSA_SDA

Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "B" SMBus Connections

PP3V3_S0

SMC
U4900
(MASTER)

SMBUS_SMC_B_S0_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_B_S0_SDA (MAKE_BASE=TRUE)

R5260 4.7K 5% 1/16W MF-LF 402
R5261 4.7K 5% 1/16W MF-LF 402

CPU Temp
EMC1403-5: U5515
(Write: 0x98 Read: 0x99)

SMBUS_SMC_B_S0_SCL
SMBUS_SMC_B_S0_SDA

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

PP3V3_S3

SMC
U4900
(MASTER)

SMBUS_SMC_MGMT_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_MGMT_SDA (MAKE_BASE=TRUE)

R5290 4.7K 5% 1/16W MF-LF 402
R5291 4.7K 5% 1/16W MF-LF 402

Vref DACs
U2900
(Write: 0x98 Read: 0x99)

SMBUS_SMC_MGMT_SCL
SMBUS_SMC_MGMT_SDA

Margin Control
U2901
(Write: 0x30 Read: 0x31)

SMBUS_SMC_MGMT_SCL
SMBUS_SMC_MGMT_SDA

HDD Margin Ctrl.
J4501
(Write: 0xXX Read: 0xXX)

SMBUS_SMC_MGMT_SCL
SMBUS_SMC_MGMT_SDA

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K19i SMBus Connections

SYNC_MASTER=WFERRY_K19I SYNC_DATE=12/12/2008

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SCALE	SHT	OF
NONE	43	83

CPU Voltage Sense / Filter

61 11 10 7 6 PPVCORE_S0_CPU

XW5309 (SM)

CPUVSENSE_IN

R5309 4.53K 1% 1/16W MF-LF 402

SMC_CPU_VSENSE OUT 40

C5309 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS 40 41 44 45

PLACEMENT_NOTE=Place near U1000 center

Place RC close to SMC

MCP Voltage Sense / Filter

64 22 21 7 6 PPVCORE_S0_MCP

XW5359 (SM)

MCPVSENSE_IN

R5359 4.53K 1% 1/16W MF-LF 402

SMC_MCP_VSENSE OUT 40 41

C5359 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS 40 41 44 45

PLACEMENT_NOTE=Place near U1400 center

Place RC close to SMC

PBUS VOLTAGE SENSE ENABLE & FILTER

Q5315
NTUD3127CXXG
SOT-963
N-CHANNEL
P-CHANNEL

68 67 PM_SLP_S3_L_BUF (IN)

Enables PBUS VSense divider when high.

PBUSVSENS_EN_L

R5316 100K 1% 1/10W MF-LF 402

PPBUS_G3HRS5_VSENSE
MIN_LINE_WIDTH=0.20 mm
MIN_NECK_WIDTH=0.20 mm
VOLTAGE=18.5V

73 64 63 62 60 59 45 35 7 6 PPBUS_G3H

R5315 100K 1% 1/10W MF-LF 402

PBUSVSENS_EN_L_DIV

R5385 27.4K 1% 1/10W MF-LF 402

RTHEVENIN = 4573 OHMS

SMC_PBUS_VSENSE OUT 40

R5386 5.49K 1% 1/10W MF-LF 402

C5385 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS 40 41 44 45

Place RC close to SMC

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VOLTAGE SENSING

SYNC_MASTER=K24_MLB SYNC_DATE=02/05/2009

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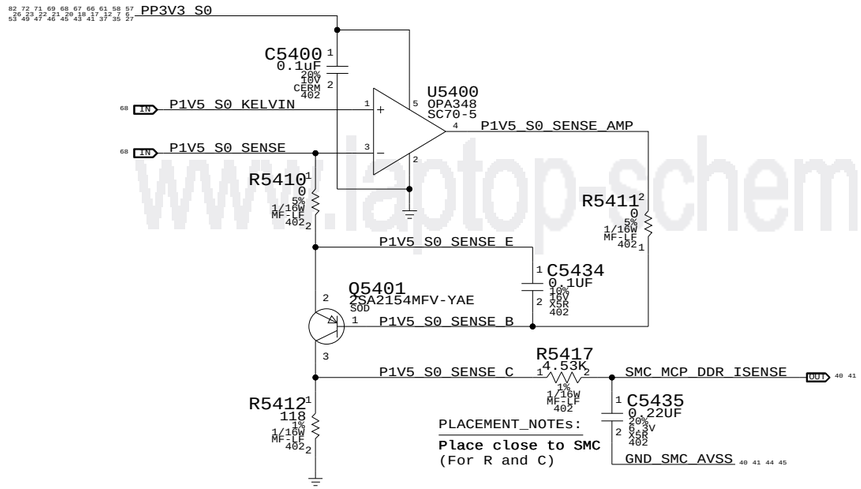
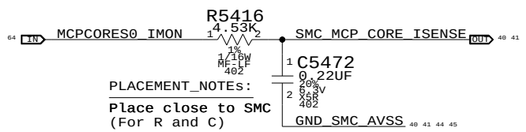
SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE: NONE	SHT 44 OF 83	

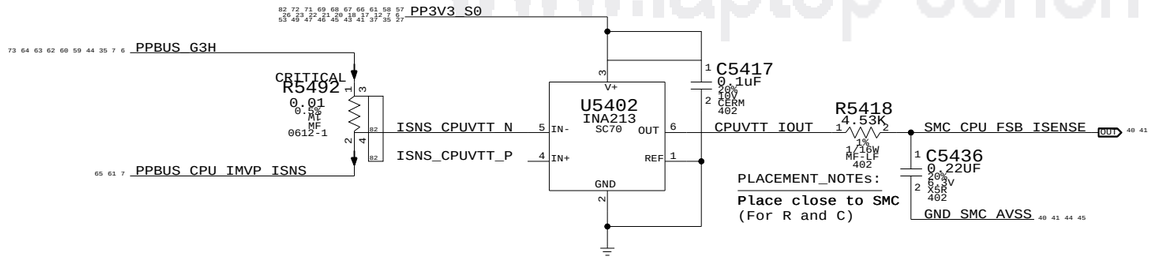
MCP MEM VDD Current Sense / Filter



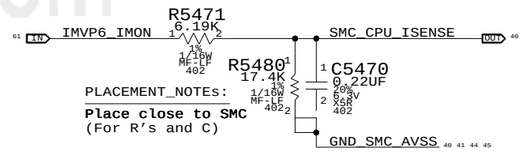
MCP VCore Current Sense Filter



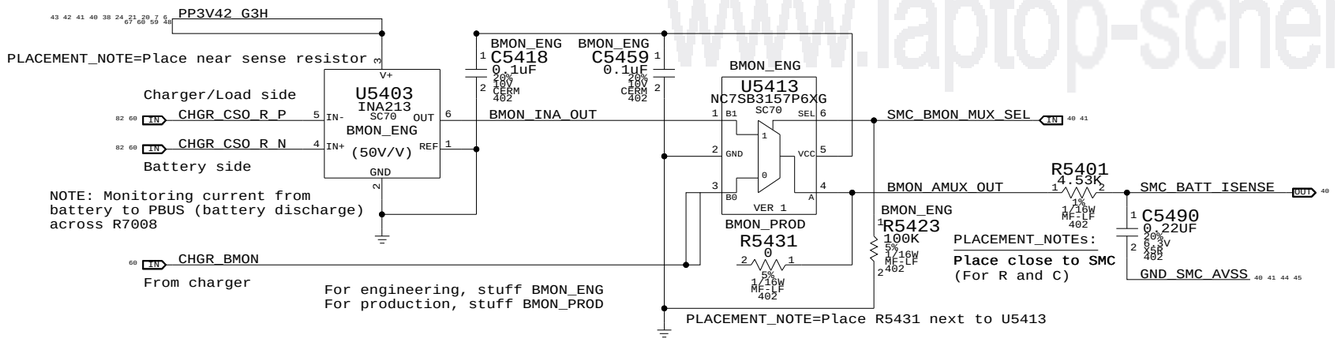
MCP/CPU 1.05V AND CPU VCore High-Side Current Sense / Filter



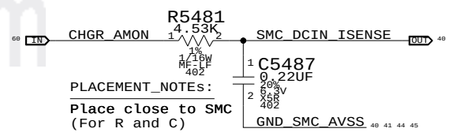
CPU VCore Load Side Current Sense / Filter



Battery (BMON) Current Sense, MUX & Filter



DC-IN (AMON) Current Sense Filter



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Current Sensing

SYNC_MASTER=WFERRY_K19I SYNC_DATE=12/16/2008

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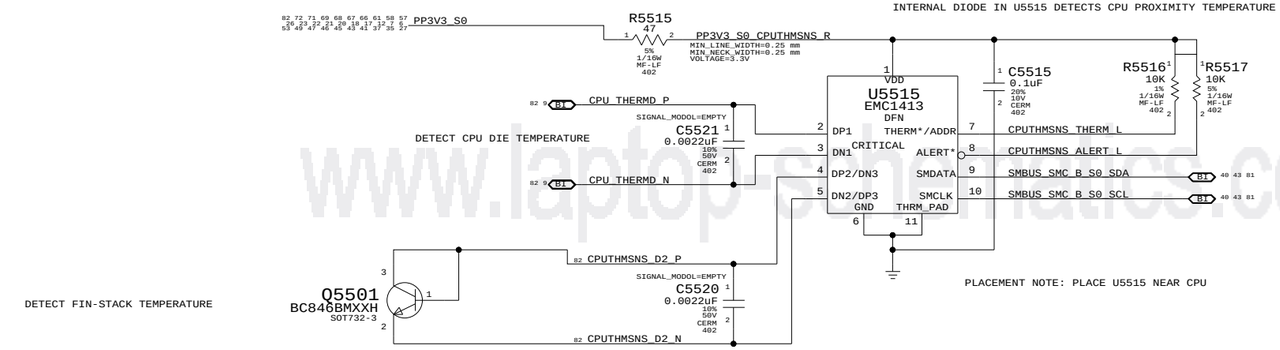
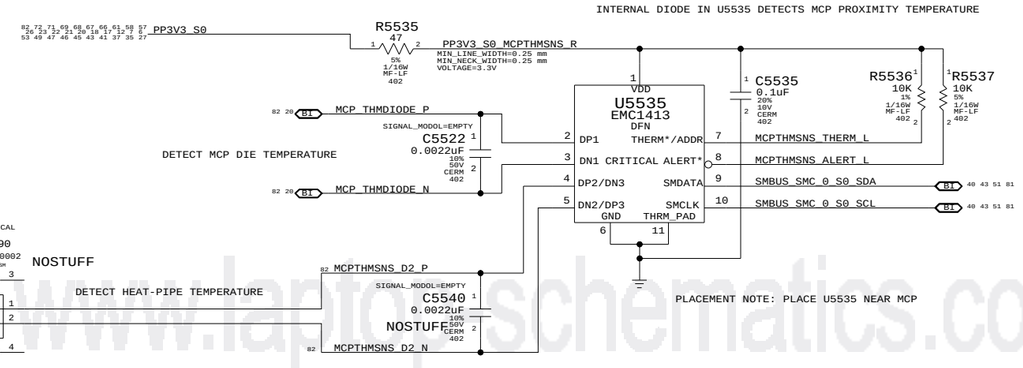
CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



REPLACED 518S0521 WITH 518S0519

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Thermal Sensors

SYNC_MASTER=K24_MLB SYNC_DATE=02/05/2009

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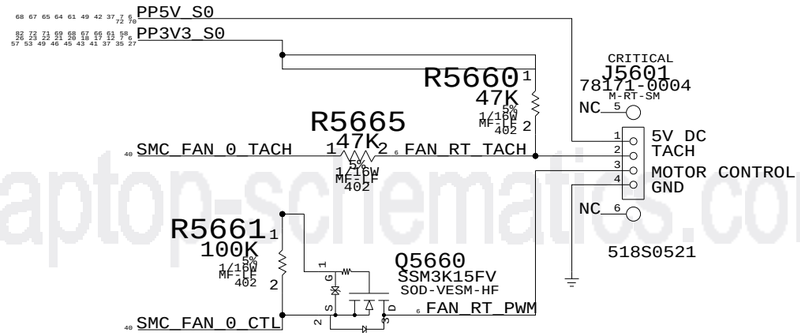

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Fan

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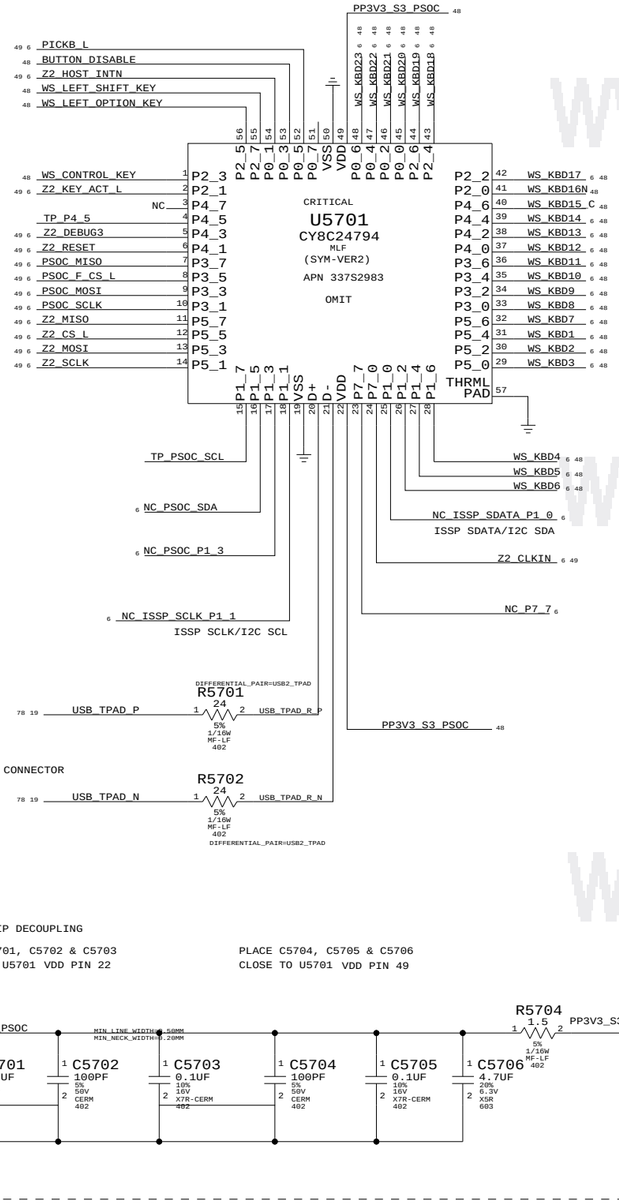
D	051-7903	A
SCALE	SHT	OF
NONE	47	83

PSOC USB CONTROLLER

USB INTERFACES TO MLB
SPI HOST TO Z2

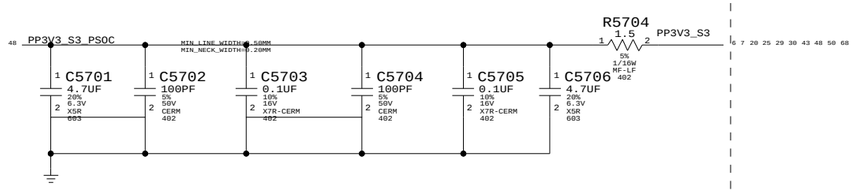
TRACKPAD PICK BUTTONS
KEYBOARD SCANNER



U5701 CHIP DECOUPLING

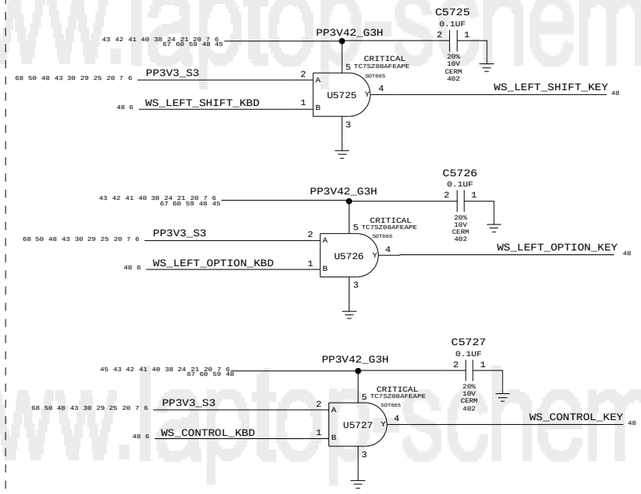
PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

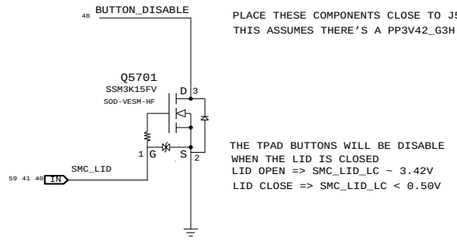


IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA 80UA	2.55 KOHM	0.0255 V 0.204 V	0.255E-6 W 16.32E-6 W
3V3 LDO	VDD VOUT	60MA MAX 60MA MAX	10 OHM 0.2 OHM	0.6 V 0.012 V	36E-3 W 0.72E-3 W
PSOC	VDD	8MA (TYP) 14MA (MAX)	1.5 OHM	0.012 V 0.021 V	96E-6 W 294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

ISOLATION CIRCUIT



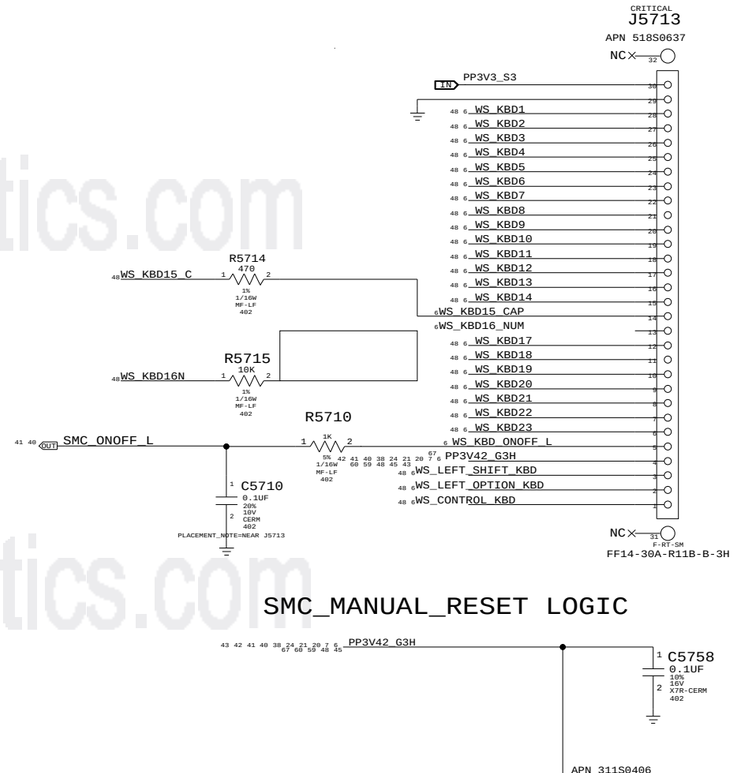
TPAD BUTTONS DISABLE



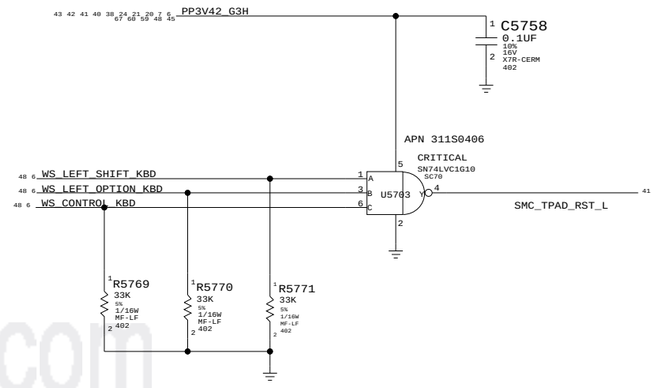
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0406	311S0447		ALL	NXP PART AS ALTERNATE

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WELLSPRING 1

SYNC_MASTER=K24_MLB SYNC_DATE=02/05/2009

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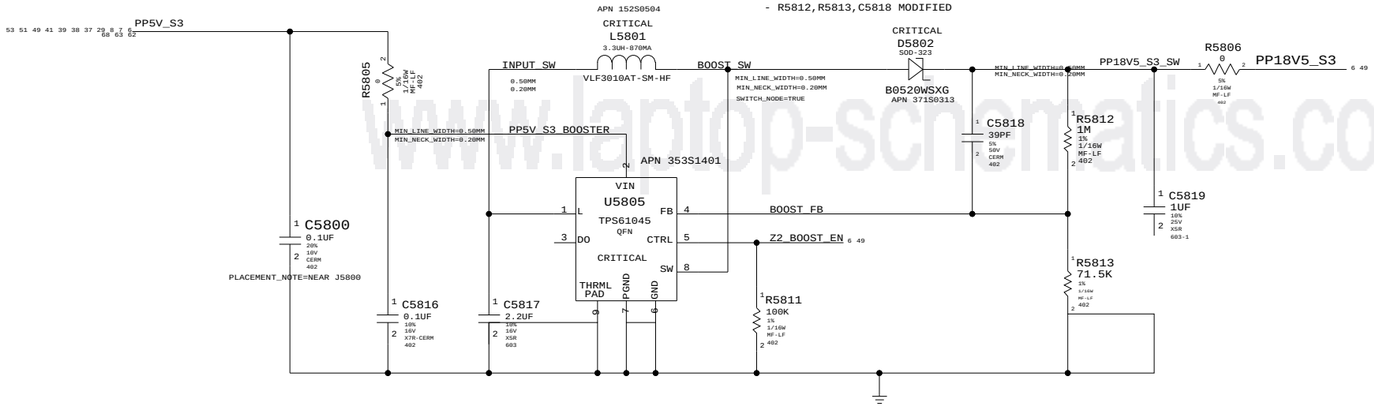
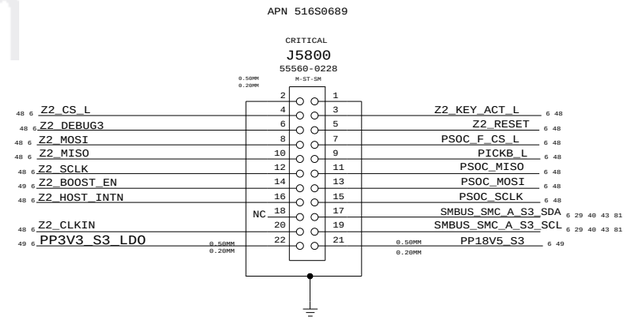
D	051-7903	A
SCALE: NONE	SHT 48 OF 83	

BOOSTER +18.5VDC FOR SENSORS

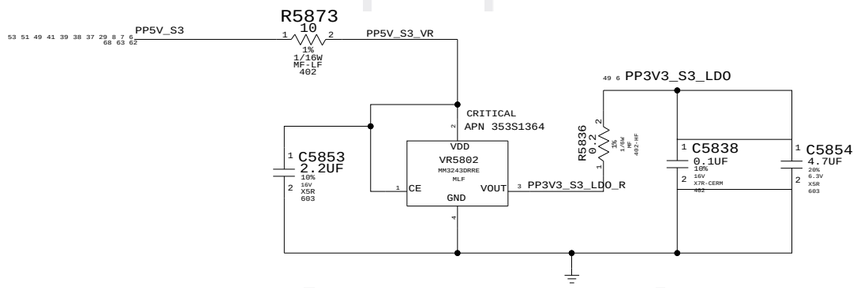
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



3V3 LDO FOR IPD



KEYBOARD BACKLIGHT DRIVNG AND DETECTION

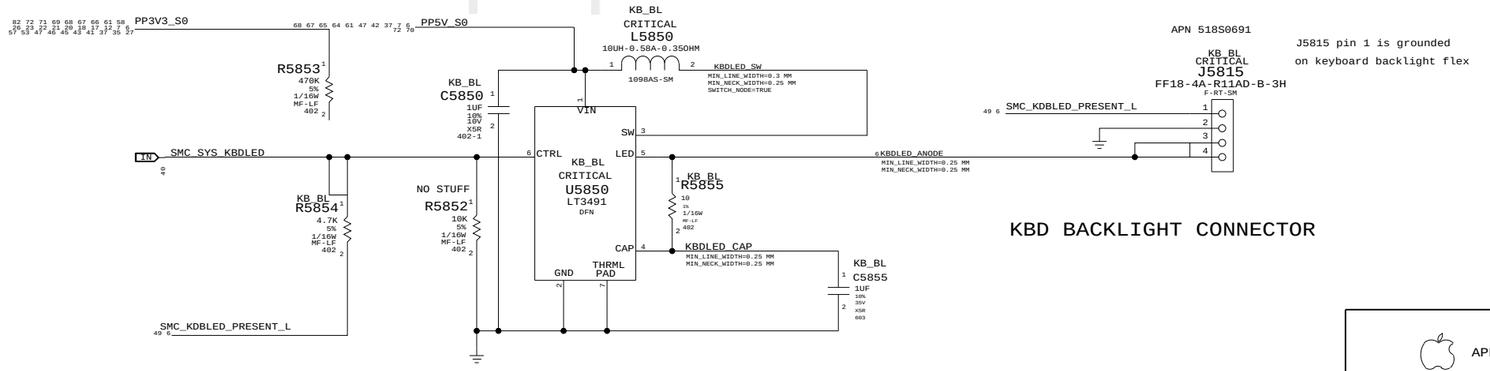
To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

LOW = keyboard backlight present

HIGH= keyboard backlight not present

BOM OPTION: KBDLED_YES
TURNED ON FOR BEST MLB CONFIG

R5853 ALWAYS PRESENT



APN 518S0691

J5815 pin 1 is grounded on keyboard backlight flex

KBD BACKLIGHT CONNECTOR

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WELLSPRING 2

SYNC_MASTER=K24_MLB SYNC_DATE=02/25/2009

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SCALE: NONE	SHT 49 OF 83	

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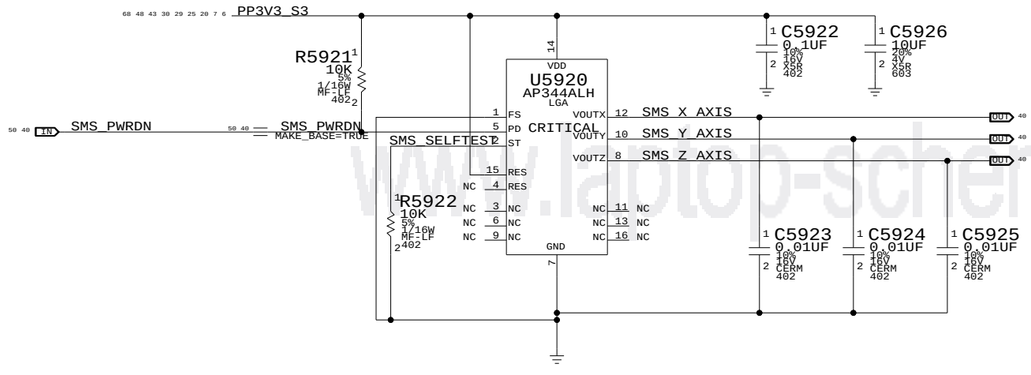
Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation

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Sudden Motion Sensor (SMS)

SYNC_MASTER=K19_MLB SYNC_DATE=02/05/2009

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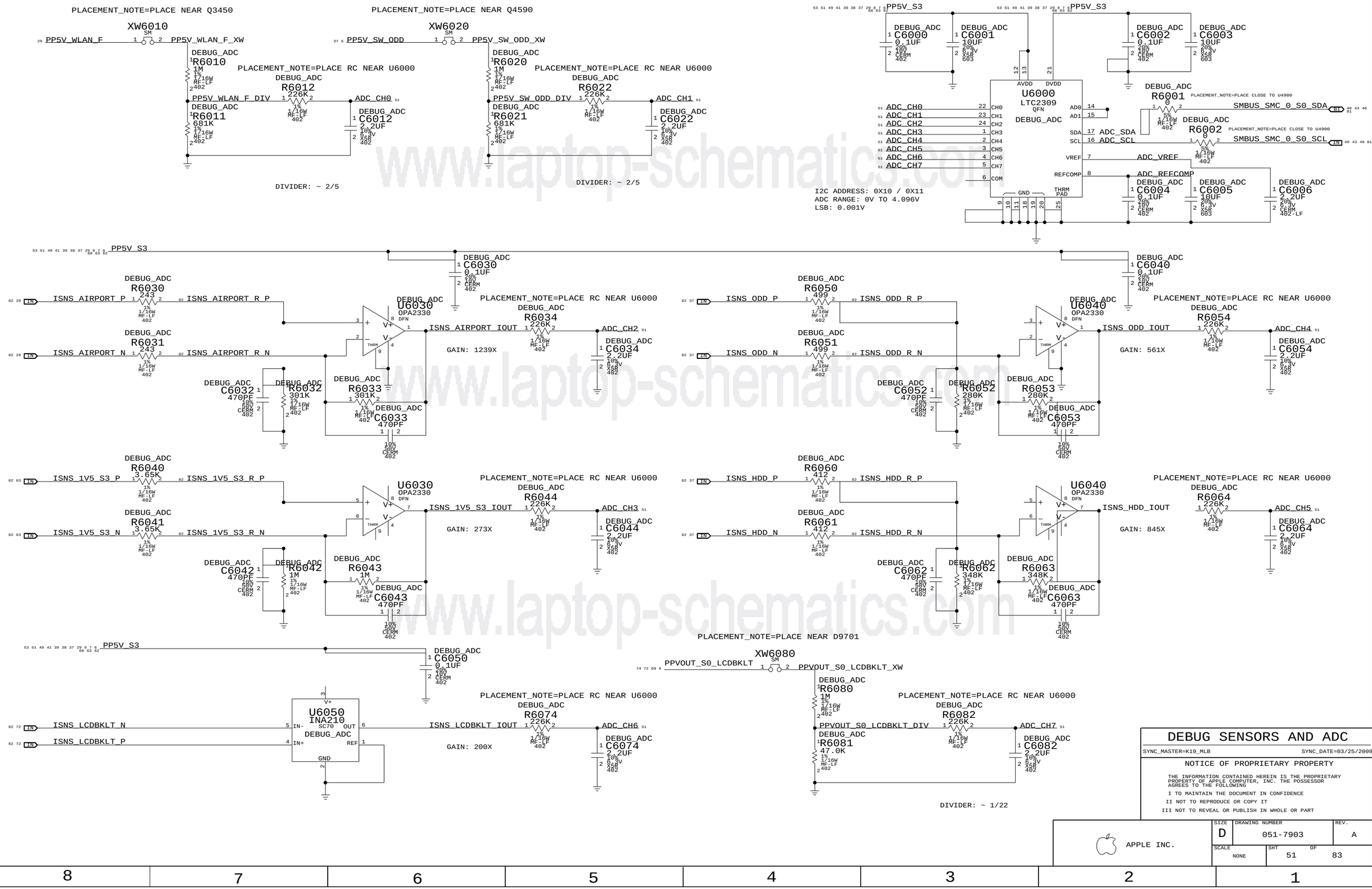
SCALE: NONE	SHT 50 OF 83	


PLACEMENT_NOTE=PLACE NEAR Q3450
XW6010
PP5V_WLAN_F
PP5V_WLAN_F_XW
R6010 1M
R6011 681K
PLACEMENT_NOTE=PLACE RC NEAR U6000
R6012 226K
PP5V_WLAN_F_DIV
ADC_CH0
C6012 2.2UF
DIVIDER: ~ 2/5
PLACEMENT_NOTE=PLACE NEAR Q4590
XW6020
PP5V_SW_ODD
PP5V_SW_ODD_XW
R6020 1M
R6021 681K
PLACEMENT_NOTE=PLACE RC NEAR U6000
R6022 226K
PP5V_SW_ODD_DIV
ADC_CH1
C6022 2.2UF
DIVIDER: ~ 2/5
PP5V_S3
C6000 0.1UF
C6001 10UF
C6002 0.1UF
C6003 10UF
U6000
LTC2309
QFN
AVDD
DVDD
GND
THRM PAD
ADC_CH0
ADC_CH1
ADC_CH2
ADC_CH3
ADC_CH4
ADC_CH5
ADC_CH6
ADC_CH7
COM
R6001 0
SMBUS_SMC_0_S0_SDA
R6002 0
SMBUS_SMC_0_S0_SCL
PLACEMENT_NOTE=PLACE CLOSE TO U4900
ADC_SDA
ADC_SCL
ADC_VREF
ADC_REFCOMP
C6004 0.1UF
C6005 10UF
C6006 2.2UF
I2C ADDRESS: 0X10 / 0X11
ADC RANGE: 0V TO 4.096V
LSB: 0.001V
R6030 243
R6031 243
ISNS_AIRPORT_P
ISNS_AIRPORT_N
ISNS_AIRPORT_R_P
ISNS_AIRPORT_R_N
U6030
OPA2330
DFN
ISNS_AIRPORT_IOUT
R6034 226K
ADC_CH2
C6034 2.2UF
GAIN: 1239X
R6032 301K
C6032 470PF
R6033 301K
C6033 470PF
C6030 0.1UF
R6050 499
R6051 499
ISNS_ODD_P
ISNS_ODD_N
ISNS_ODD_R_P
ISNS_ODD_R_N
U6040
OPA2330
DFN
ISNS_ODD_IOUT
R6054 226K
ADC_CH4
C6054 2.2UF
GAIN: 561X
R6052 280K
C6052 470PF
R6053 280K
C6053 470PF
C6040 0.1UF
R6040 3.65K
R6041 3.65K
ISNS_1V5_S3_P
ISNS_1V5_S3_N
ISNS_1V5_S3_R_P
ISNS_1V5_S3_R_N
U6030
OPA2330
DFN
ISNS_1V5_S3_IOUT
R6044 226K
ADC_CH3
C6044 2.2UF
GAIN: 273X
R6042 1M
C6042 470PF
R6043 1M
C6043 470PF
C6030 0.1UF
R6060 412
R6061 412
ISNS_HDD_P
ISNS_HDD_N
ISNS_HDD_R_P
ISNS_HDD_R_N
U6040
OPA2330
DFN
ISNS_HDD_IOUT
R6064 226K
ADC_CH5
C6064 2.2UF
GAIN: 845X
R6062 348K
C6062 470PF
R6063 348K
C6063 470PF
C6040 0.1UF
PP5V_S3
C6050 0.1UF
U6050
INA210
SC70
ISNS_LCDBKLT_N
ISNS_LCDBKLT_P
ISNS_LCDBKLT_IOUT
R6074 226K
ADC_CH6
C6074 2.2UF
GAIN: 200X
PLACEMENT_NOTE=PLACE NEAR D9701
XW6080
PPVOUT_S0_LCDBKLT
PPVOUT_S0_LCDBKLT_XW
R6080 1M
R6081 47.0K
PPVOUT_S0_LCDBKLT_DIV
R6082 226K
ADC_CH7
C6082 2.2UF
DIVIDER: ~ 1/22
DEBUG SENSORS AND ADC
SYNC_MASTER=K19_MLB
SYNC_DATE=03/25/2009
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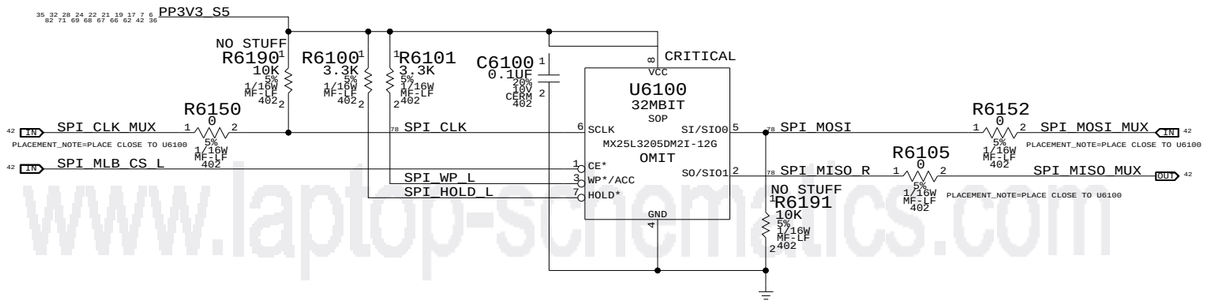
SHT 51 OF 83



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

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SPI ROM

SYNC_MASTER=K19_MLB SYNC_DATE=02/05/2009

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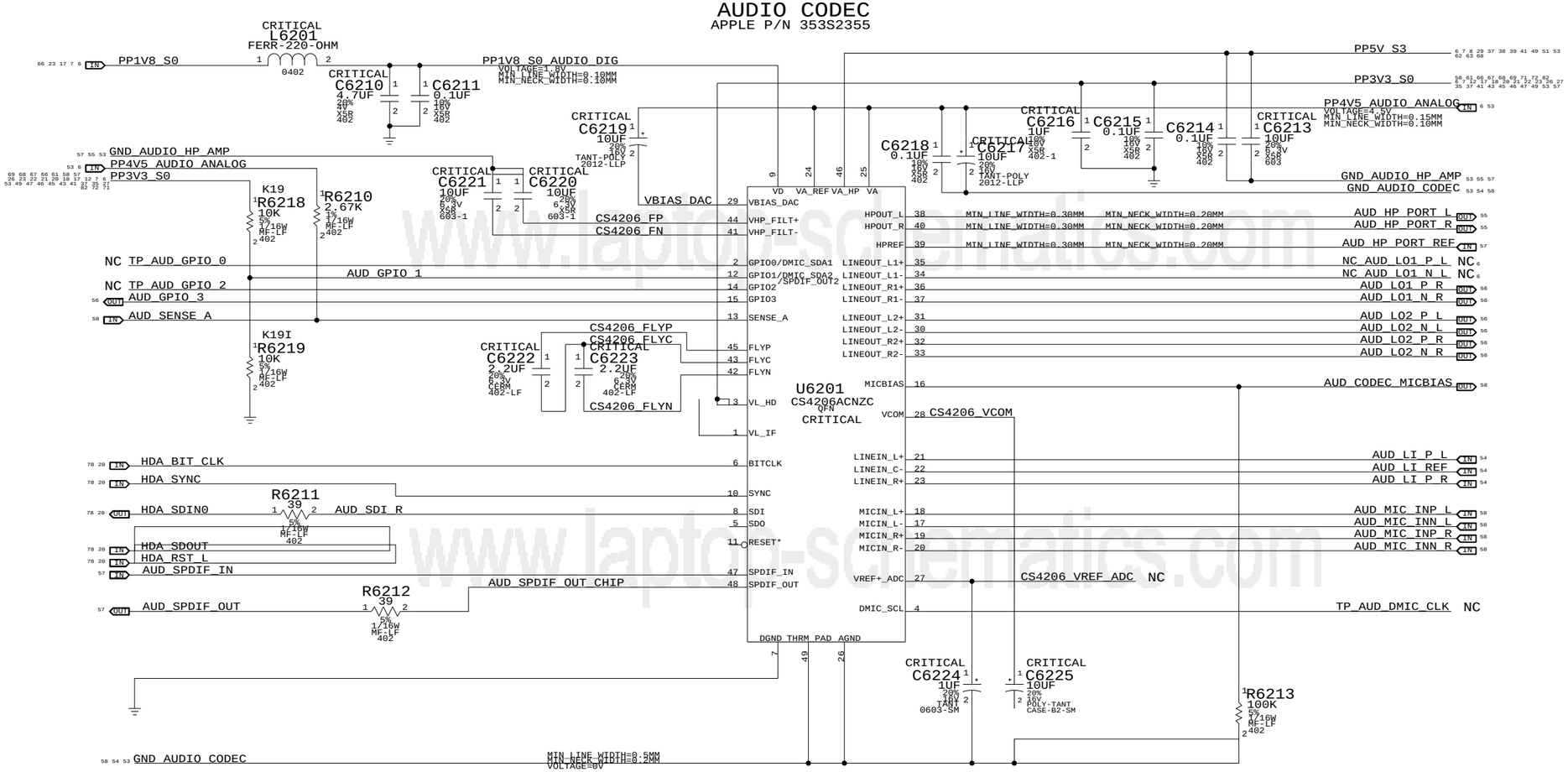
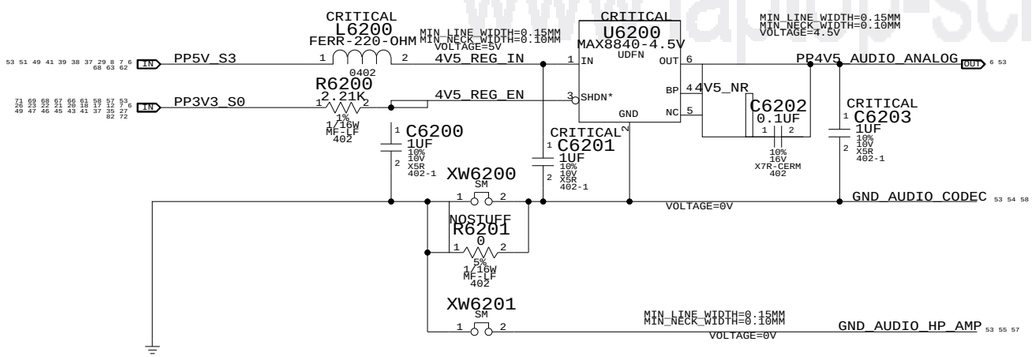
AUDIO CODEC
APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2234



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

AUDIO: CODEC/REGULATOR

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SCALE: NONE	SHT 53 OF 83	

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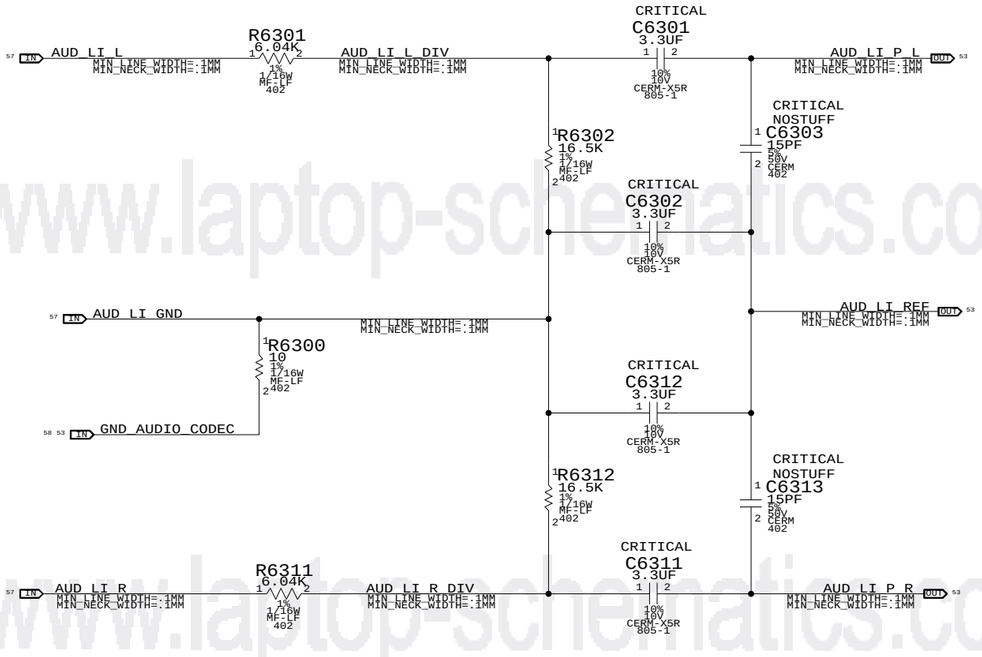
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 20K OHMS
FC = 8 HZ
VIN = 2VRMS, CODEC VIN = 1.21 VRMS



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AUDIO: LINE INPUT FILTER

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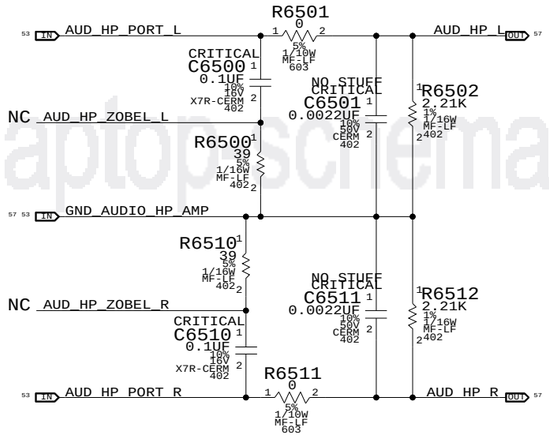
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE: NONE	SHT 54 OF 83	

ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



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AUDIO: HEADPHONE FILTER

SYNC_MASTER=K19_MLB SYNC_DATE=02/05/2009

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D	051-7903	A

SCALE	SHT	OF
NONE	55	83

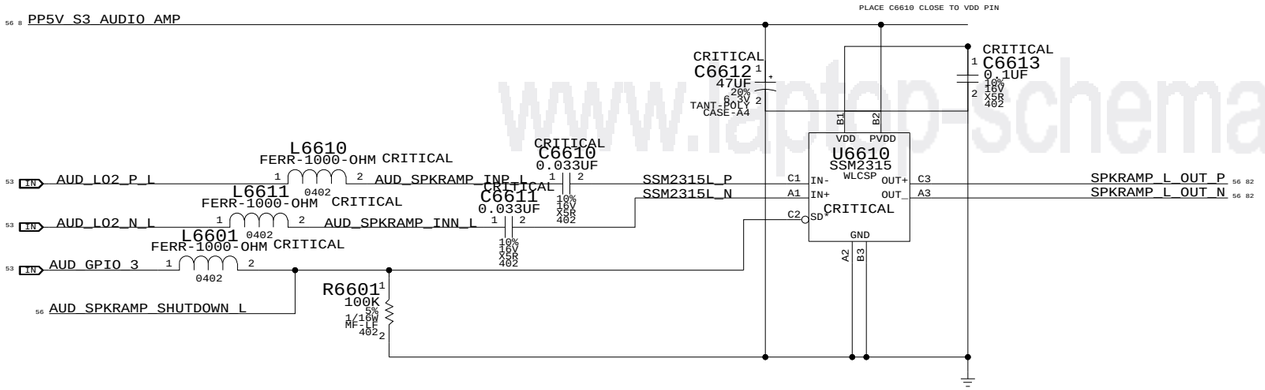
3X MONO SPEAKER AMPLIFIERS (SSM2315)

APN: 353S2500

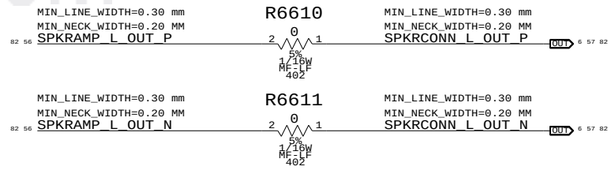
GAIN = 6DB

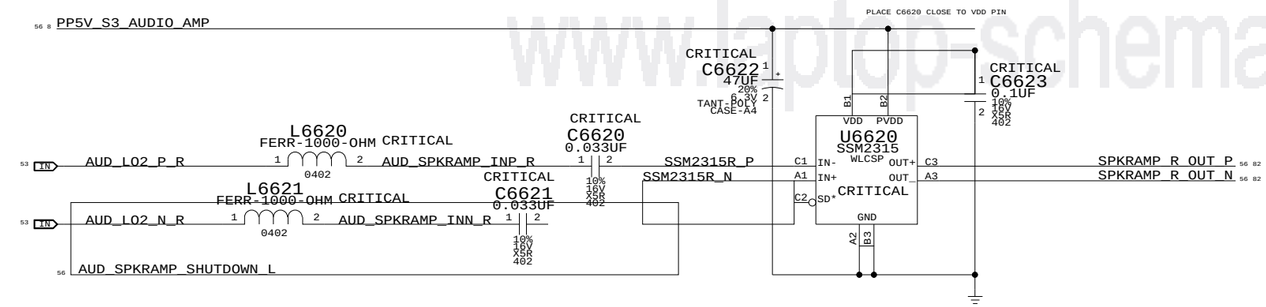
1ST ORDER FC (L&R) = 120 HZ +/- 30%

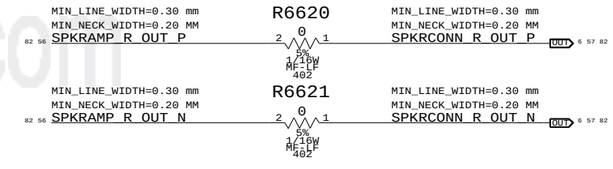
1ST ORDER FC (SUB) = 58HZ +/- 30%

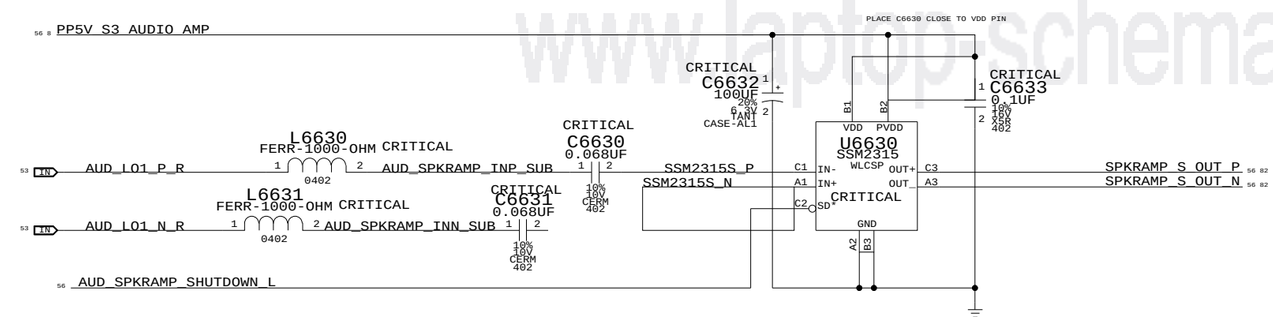


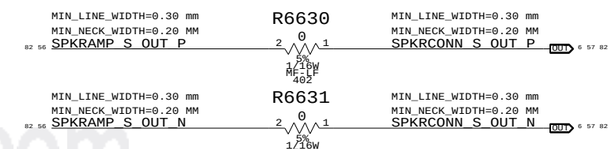
SPEAKER CHECKPOINTS











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AUDIO:SPEAKER AMP

SYNC_MASTER=K19_MLB SYNC_DATE=02/05/2009

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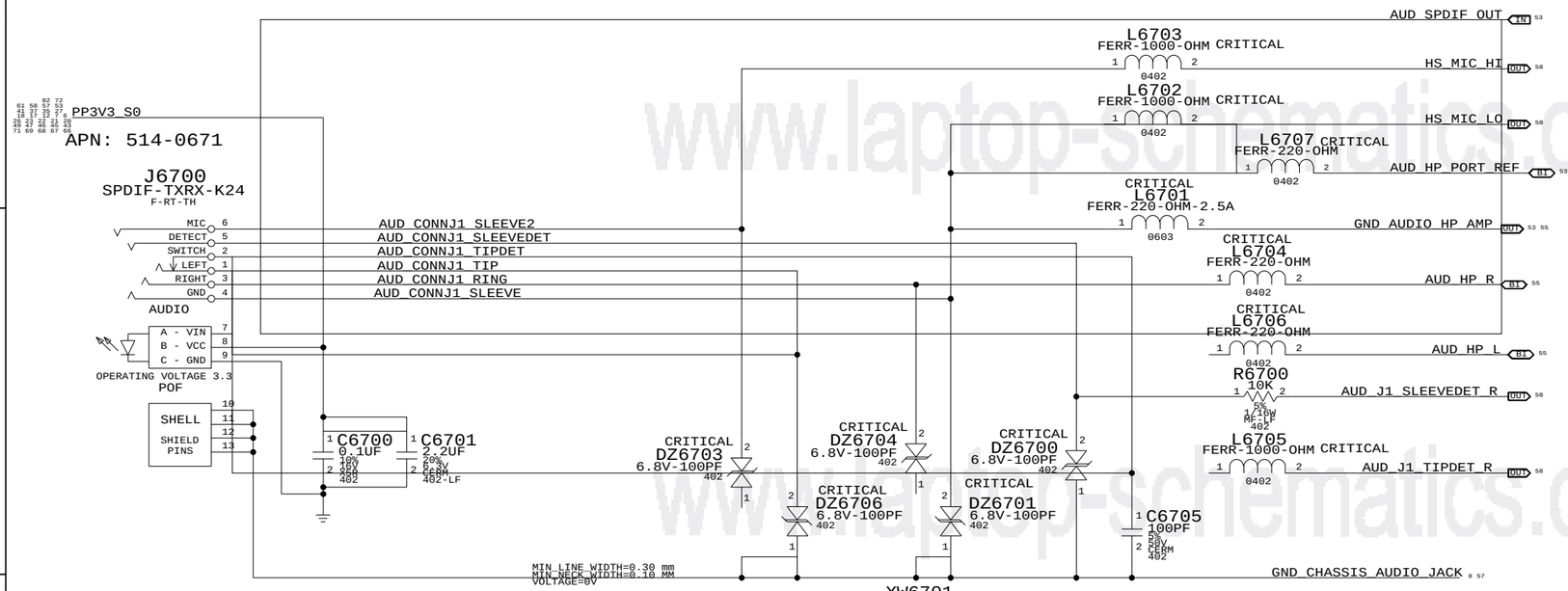
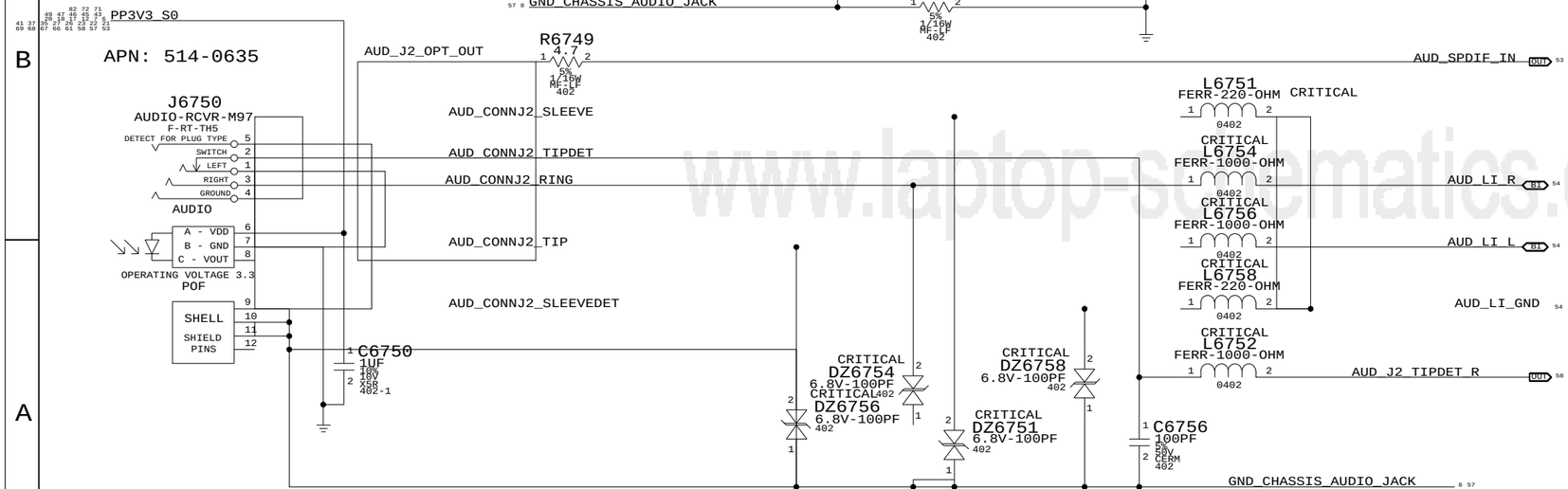
SCALE: NONE	SHT 56 OF 83	

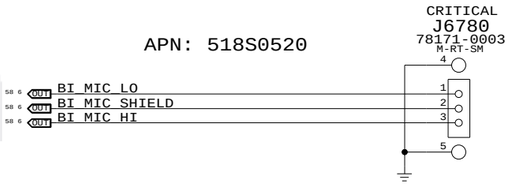
AUDIO JACK 1 LO/HP JACK, SPDIF TX





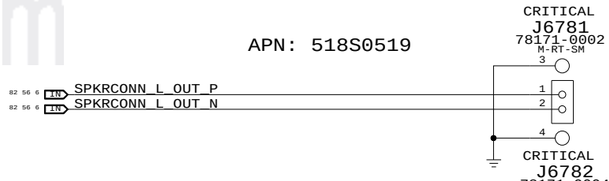
MIC CONNECTOR

APN: 518S0520

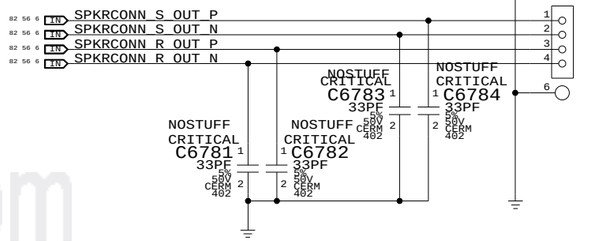


SPEAKER CONNECTOR

APN: 518S0519



APN: 518S0521



AUDIO JACK 2 LINE IN JACK, SPDIF RX

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AUDIO: JACKS

SYNC_MASTER=CASEYHARDY_K19 SYNC_DATE=03/20/2009

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D	051-7903	A
SCALE	SHT	OF
NONE	57	83

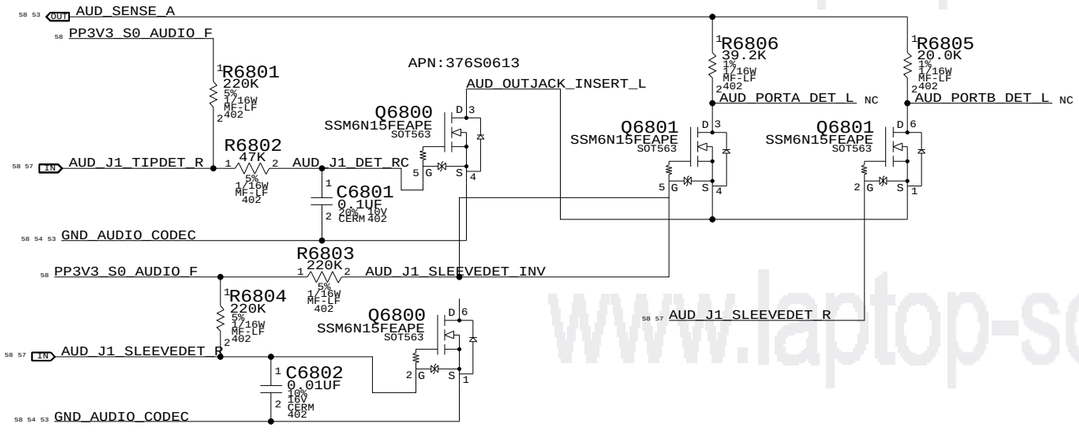
CODEC OUTPUT SIGNAL PATHS

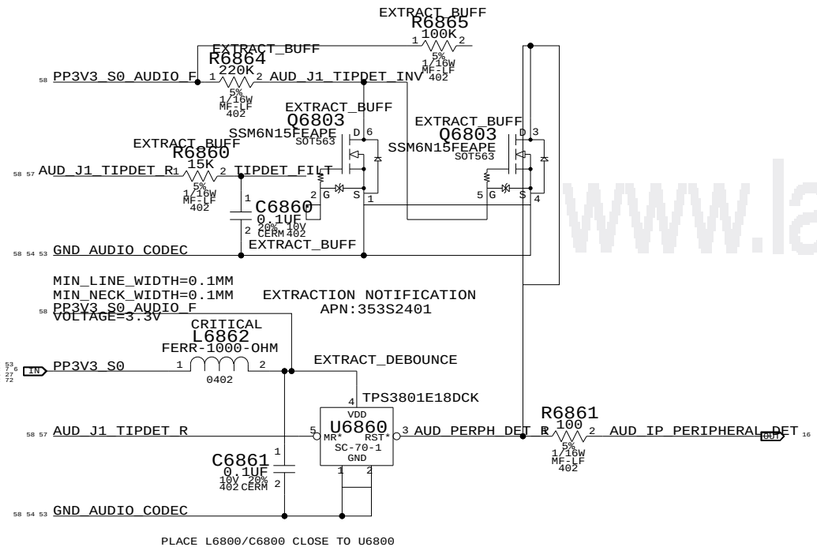
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (B)

CODEC INPUT SIGNAL PATHS

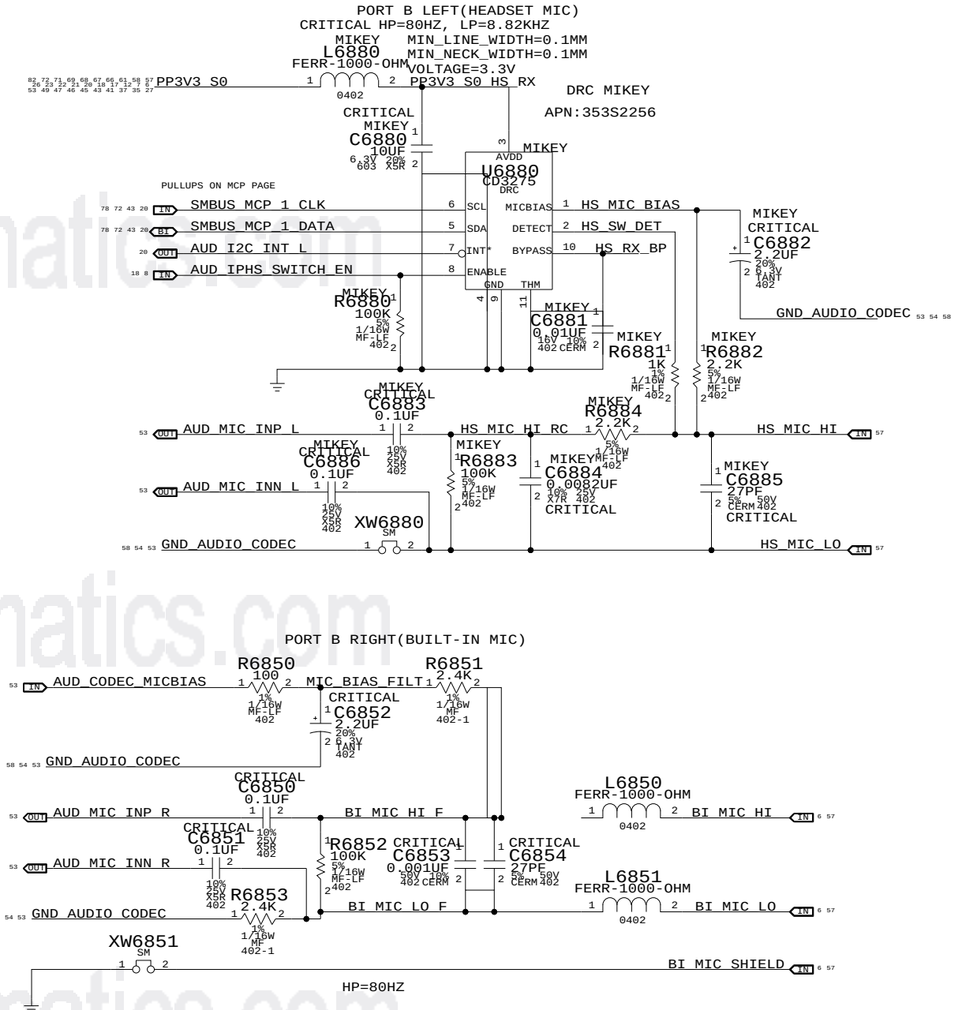
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

PORT A DETECT (HEADPHONES) PORT B DETECT(SPDIF DELEGATE)



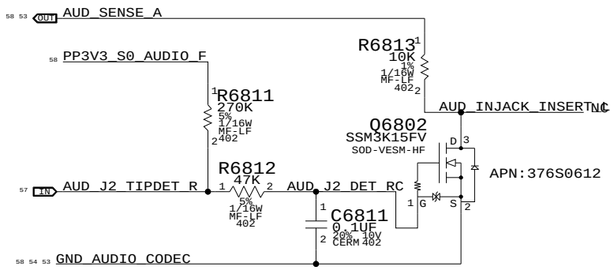


PORT B LEFT(HEADSET MIC)
CRITICAL HP=80HZ, LP=8.82KHZ
MIN_LINE_WIDTH=0.1MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=3.3V



PORT B RIGHT(BUILT-IN MIC)

PORT C DETECT (LINE-IN)



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AUDIO: JACK TRANSLATORS

SYNC_MASTER=K19_MLB SYNC_DATE=03/17/2009

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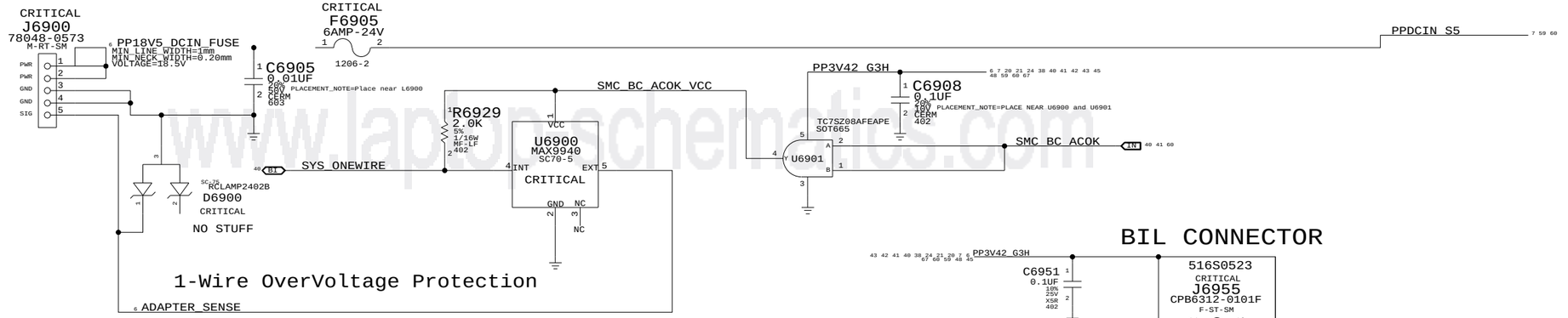
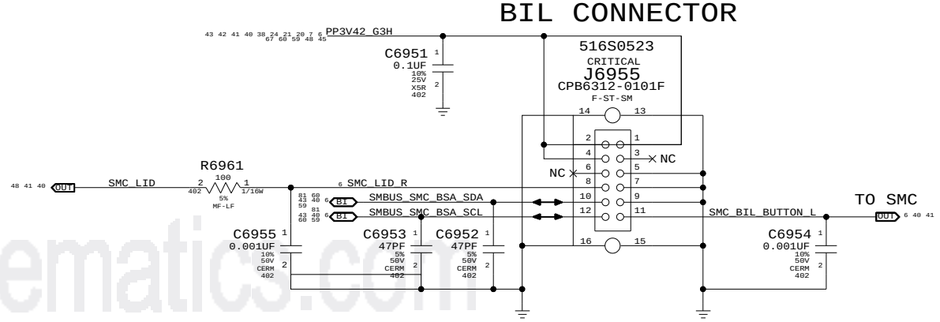
SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE: NONE	SHT 58 OF 83	

MagSafe DC Power Jack



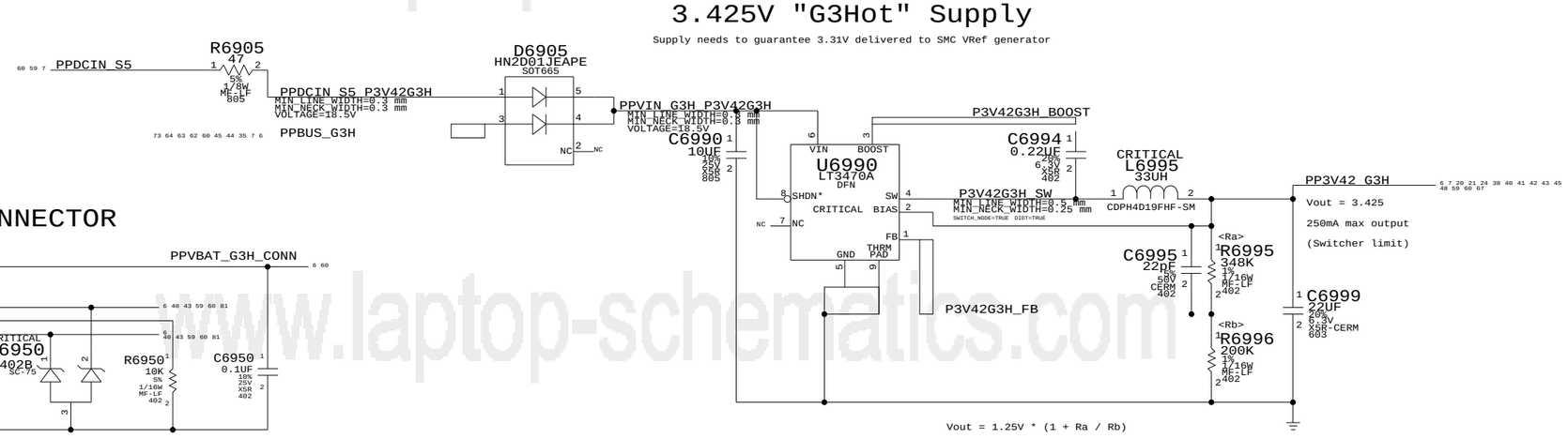
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

BIL CONNECTOR

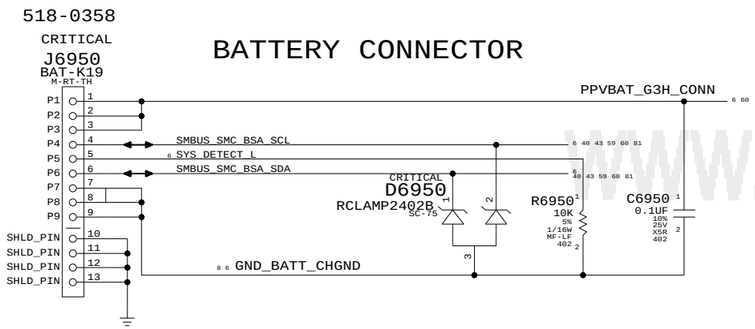


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR



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DC-In & Battery Connectors

SYNC_MASTER=K19_MLB SYNC_DATE=03/18/2009

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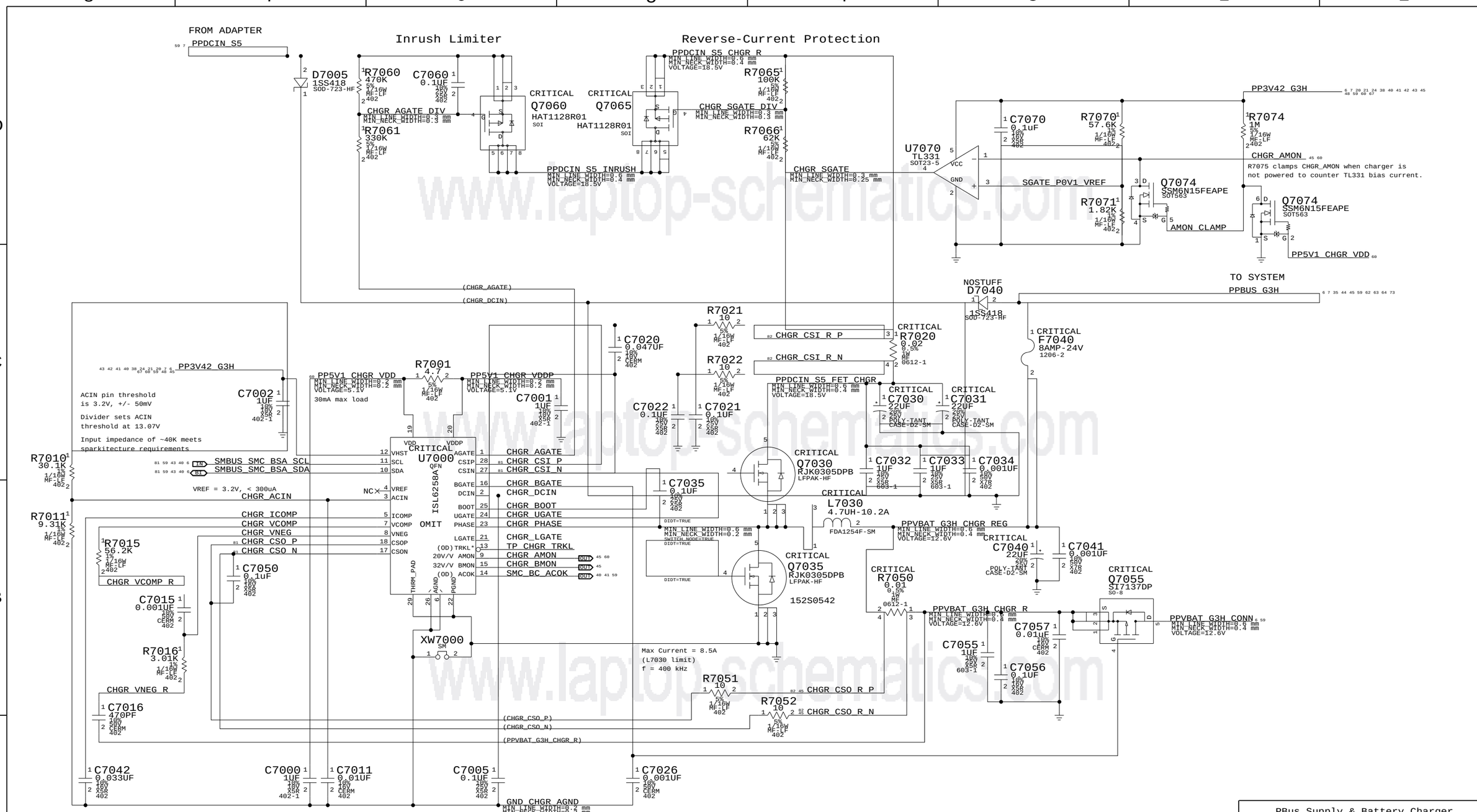
SIZE	DRAWING NUMBER	REV.
D	051-7903	A

SCALE	SHT	OF
NONE	59	83



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
353S1811	1	IC,ISL6258,BAT CHARGER,28P,4X4,QFN,L	U7000	CRITICAL	ISL6258	2S Battery Default
353S1832	1	IC,ISL6258A,BAT CHARGER,4X4MM,QFN28	U7000	CRITICAL	ISL6258A	3S Battery Default

PBus Supply & Battery Charger

SYNC_MASTER=K19_MLB SYNC_DATE=03/18/2009

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A

SCALE NONE SHT 60 OF 83

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

These caps are for Q7100

These caps are for Q7102

Place R7131 Between L7100,L7101 and CPU

NO STUFF

LAYOUT NOTE:
Place R7126 in hot spot of reg circuit.

IMVP6_PHASE1	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM	
IMVP6_BOOT1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM	
IMVP6_UGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM	
IMVP6_LGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM	
IMVP6_ISEN1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM	
IMVP6_VSUM1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	
IMVP6_VO1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	
IMVP6_VSEN_P	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM	

IMVP6_PHASE2	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM	
IMVP6_BOOT2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM	
IMVP6_UGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM	
IMVP6_LGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM	
IMVP6_ISEN2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM	
IMVP6_VSUM2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	
IMVP6_VO2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	
IMVP6_VSEN_N	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM	

IMVP6_OCSET	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	
IMVP6_VO	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	
IMVP6_DROOP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	
IMVP6_DFB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	
IMVP6_SOFT	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	
IMVP6_RBIAS	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	
IMVP6_VDIFF	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	
IMVP6_FB2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	
IMVP6_FB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	
IMVP6_COMP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	
IMVP6_VW	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	

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IMVP6 CPU VCore Regulator

SYNC_MASTER=K19_MLB SYNC_DATE=02/05/2009

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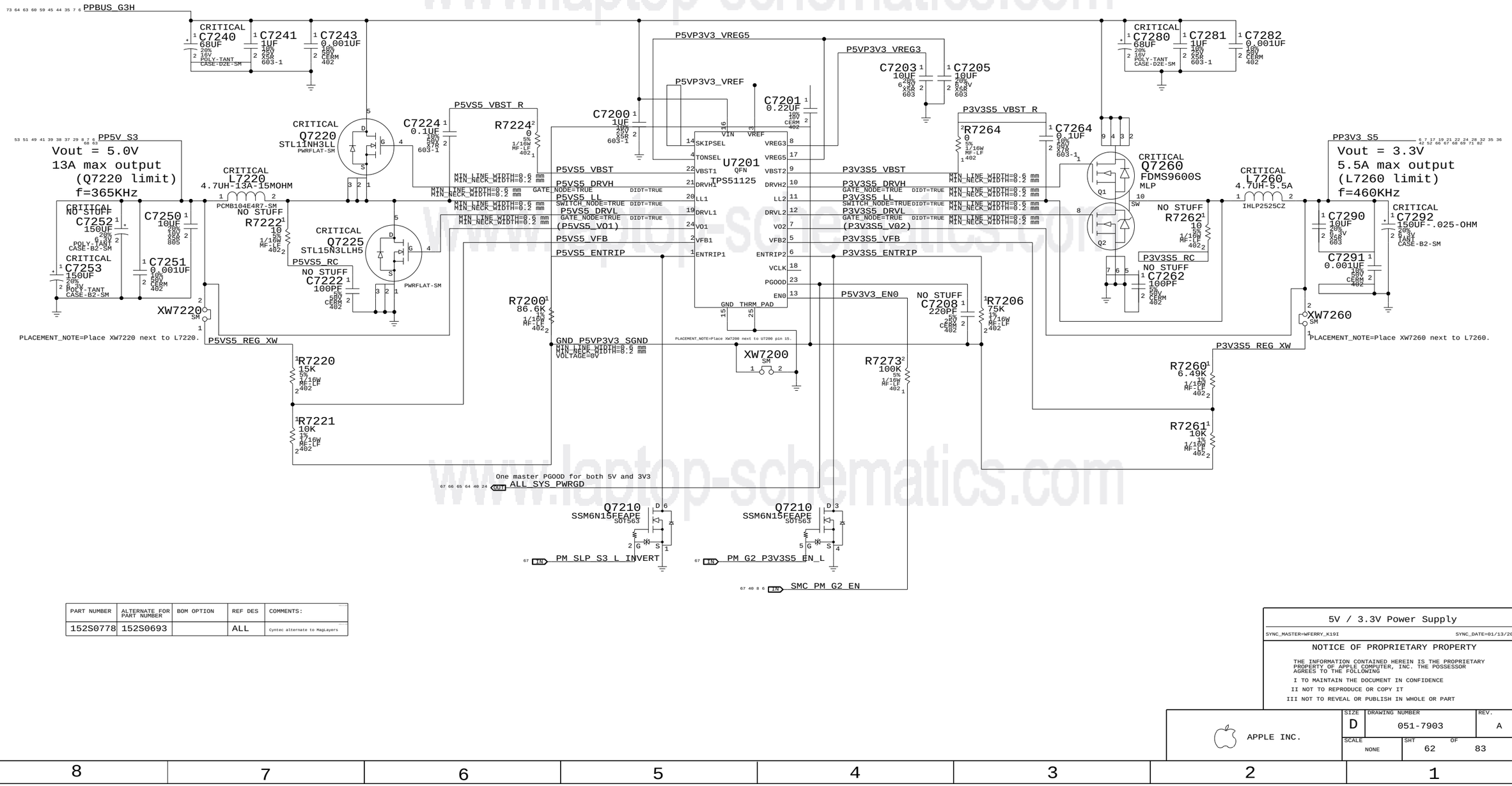
SCALE: NONE	SHT 61 OF 83	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	Cyntec alternate to MagLayers

5V / 3.3V Power Supply

SYNC_MASTER=WFERRY_K19I SYNC_DATE=01/13/2009

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SCALE: NONE SHT 62 OF 83

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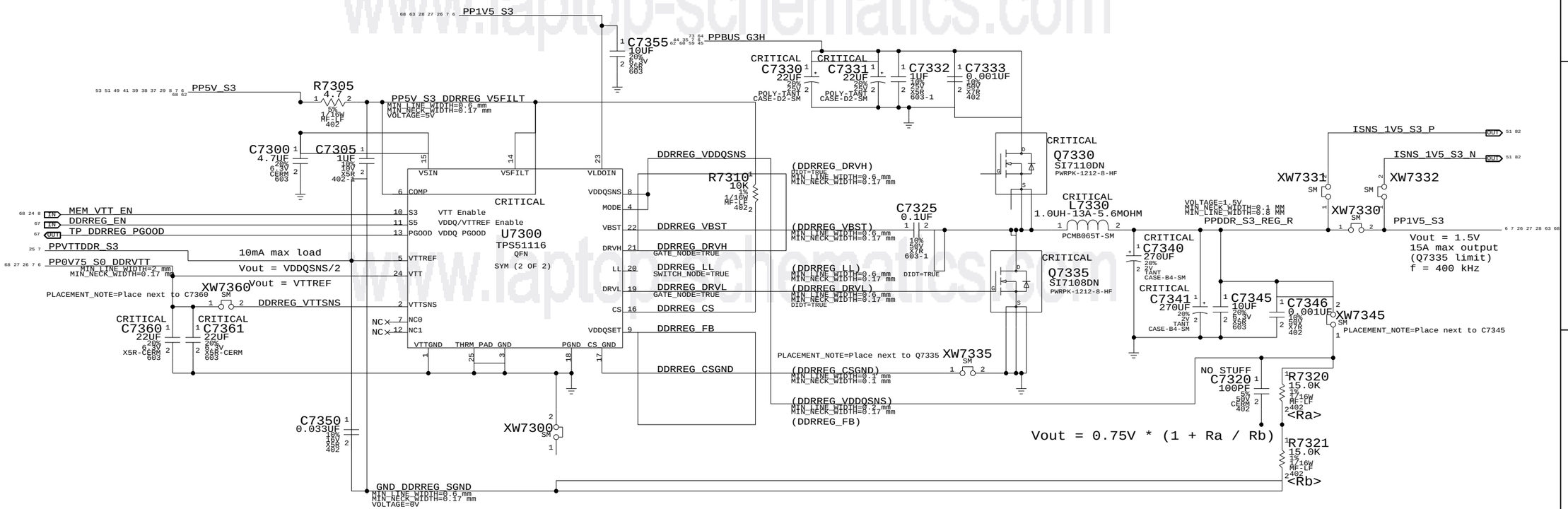

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1.5V DDR3 Supply

SYNC_MASTER=K19_MLB SYNC_DATE=02/04/2009

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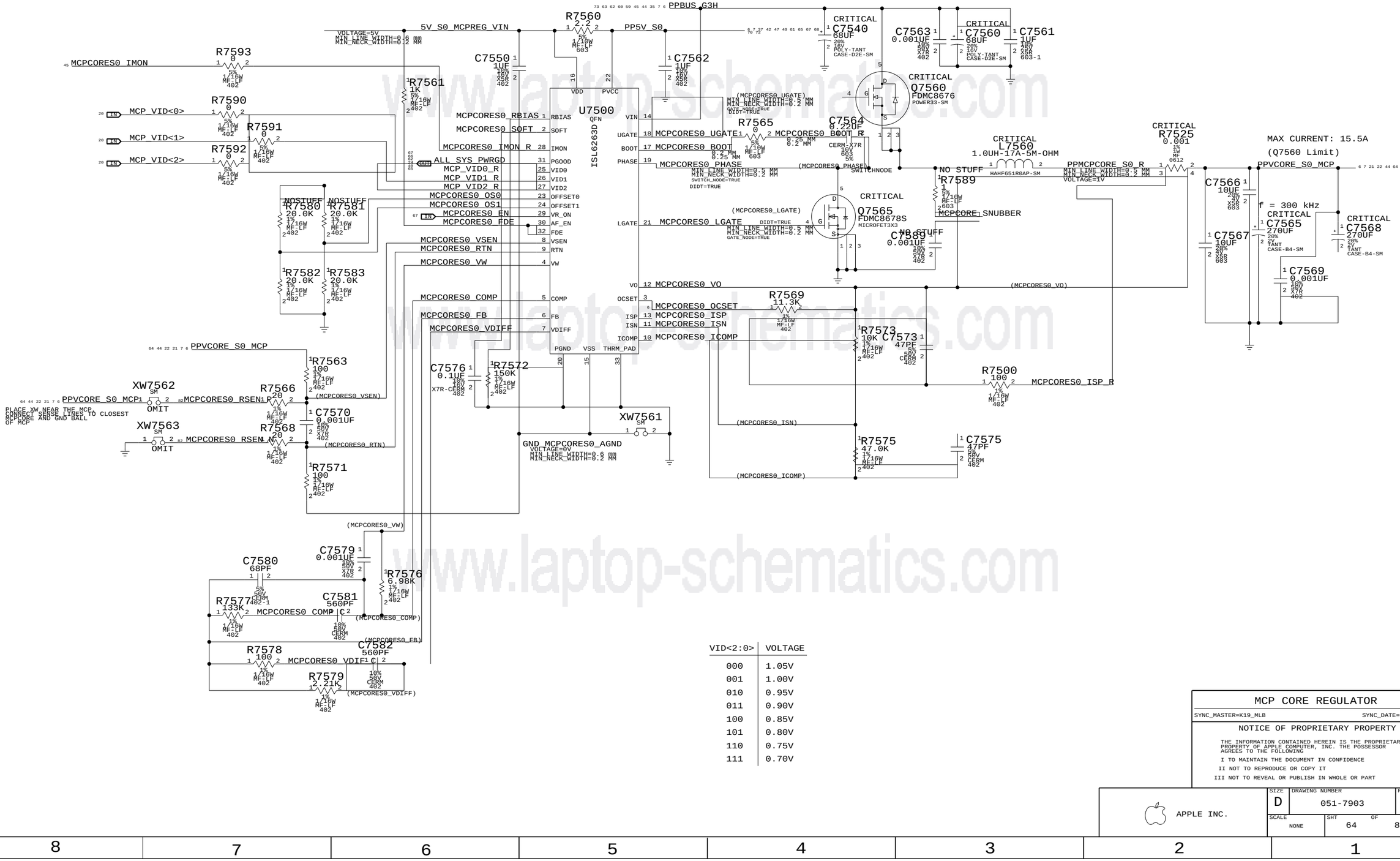
SCALE	SHT	OF
NONE	63	83



VID<2:0>	VOLTAGE
000	1.05V
001	1.00V
010	0.95V
011	0.90V
100	0.85V
101	0.80V
110	0.75V
111	0.70V

MCP CORE REGULATOR

SYNC_MASTER=K19_MLB SYNC_DATE=02/03/2009

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SCALE: NONE	SHT 64 OF 83	

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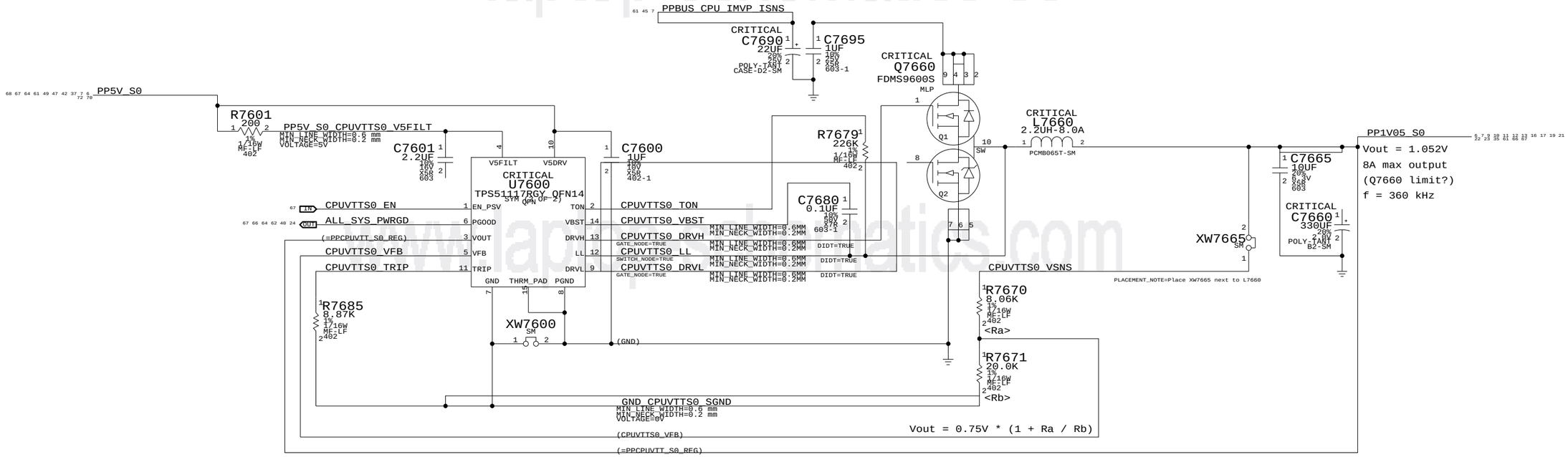

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M99 differences from last sync on 12/03/07 to T18 MLB:
1. Tied THERMAL_PAD to PGND. GND and THERMAL_PAD disconnected.

CPU VTT Power Supply

SYNC_MASTER=(K19_MLB) SYNC_DATE=(12/05/2008)

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SIZE	DRAWING NUMBER	REV.
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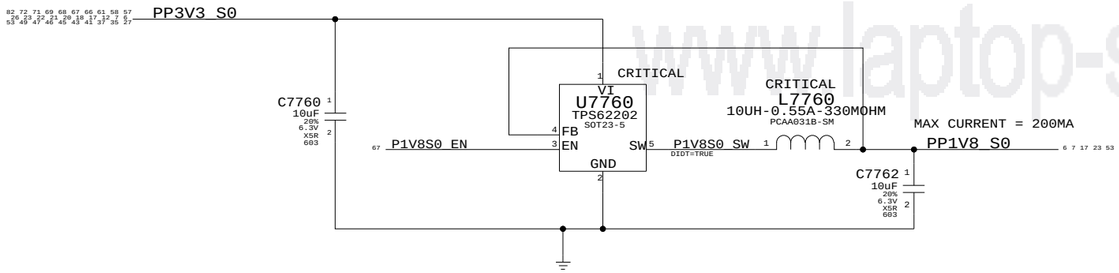
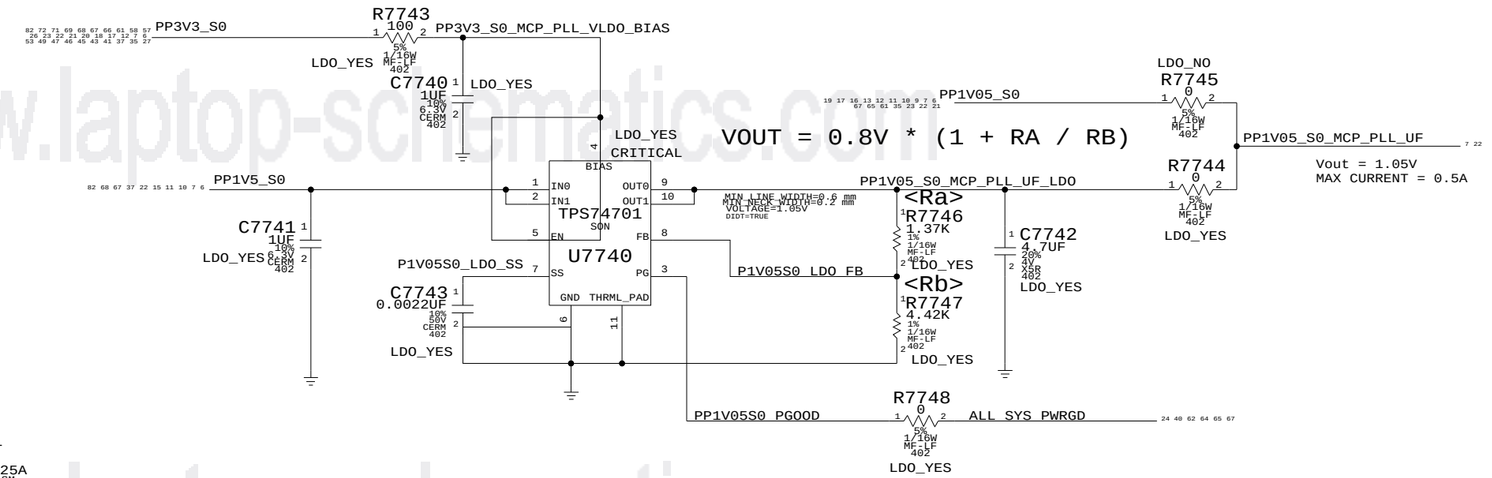
SCALE: NONE	SHT 65 OF 83	

1.8V S0 SWITCHER

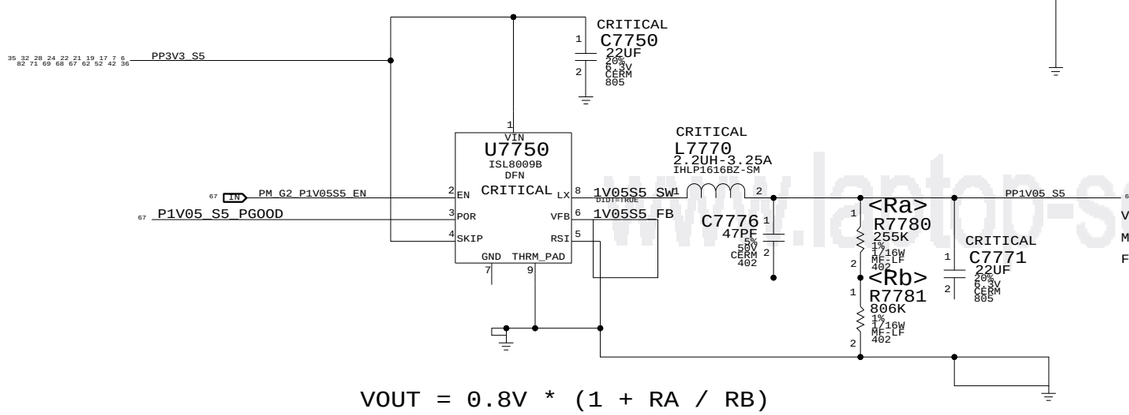


1.05V S0 PLL LDO



VOUT = 0.8V * (1 + RA / RB)

MCP 1.05V S5 (AUXC) SUPPLY



VOUT = 0.8V * (1 + RA / RB)

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MISC POWER SUPPLIES

SYNC_MASTER=K24_MLB SYNC_DATE=02/25/2009

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SCALE	SHT	OF
NONE	66	83

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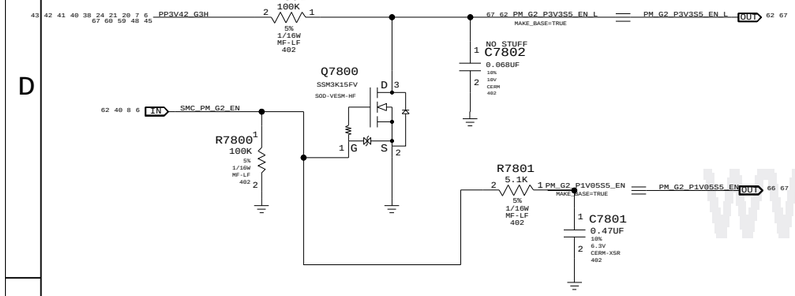
3.3V 1.05V S5 ENABLE

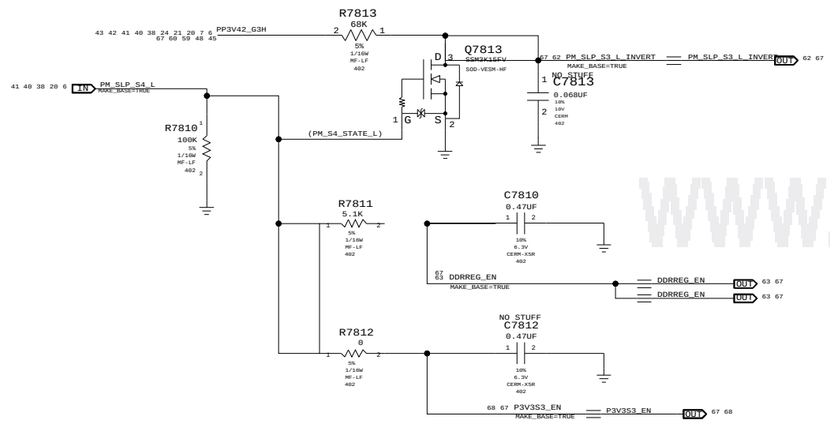


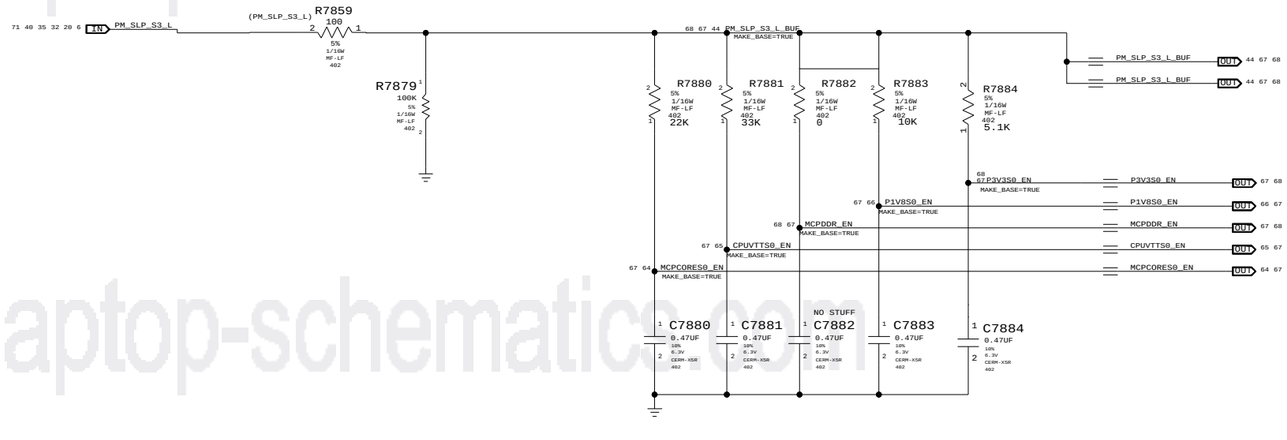
Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

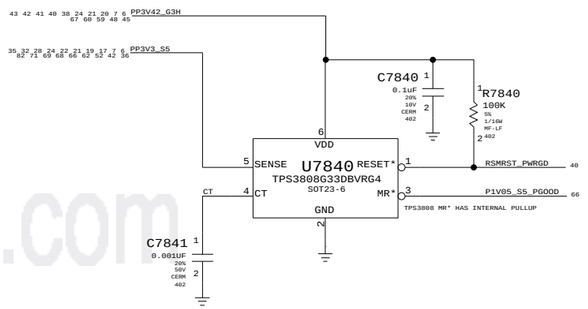
3.3V_S0, 1.8V_S0 ENABLE
MCPDDR, CPUVTT,MCPCORES0 ENABLE
1.5V S0 AND 1.05V S0 ENABLE

S3 ENABLE

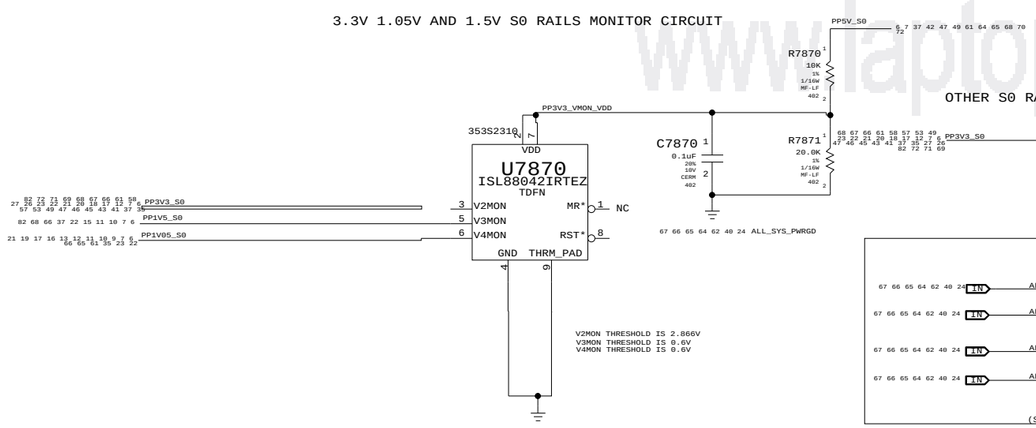




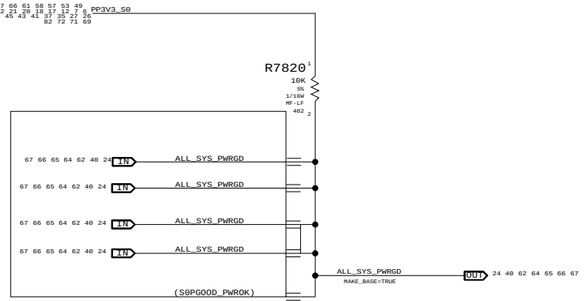
VOLTAGE MONITOR



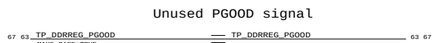
3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT



OTHER S0 RAILS PGOOD



Unused PGOOD signal



POWER SEQUENCING

SYNC_MASTER=K24_MLB SYNC_DATE=02/05/2009

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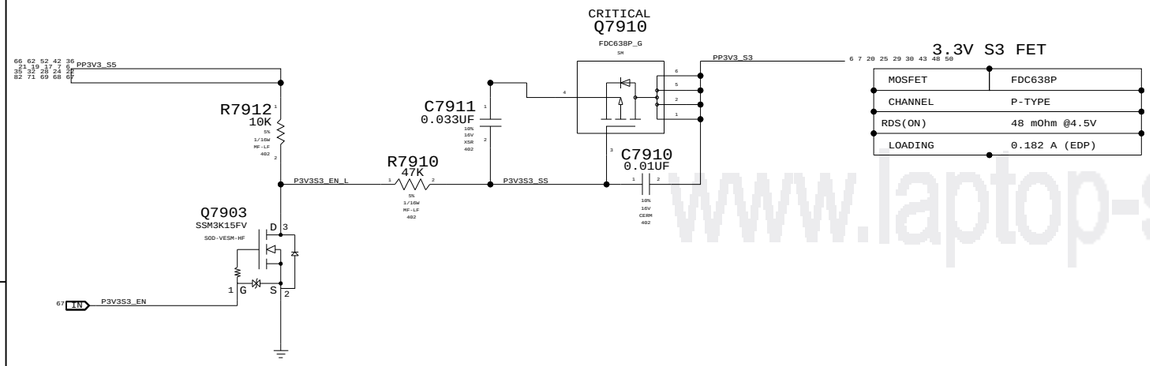
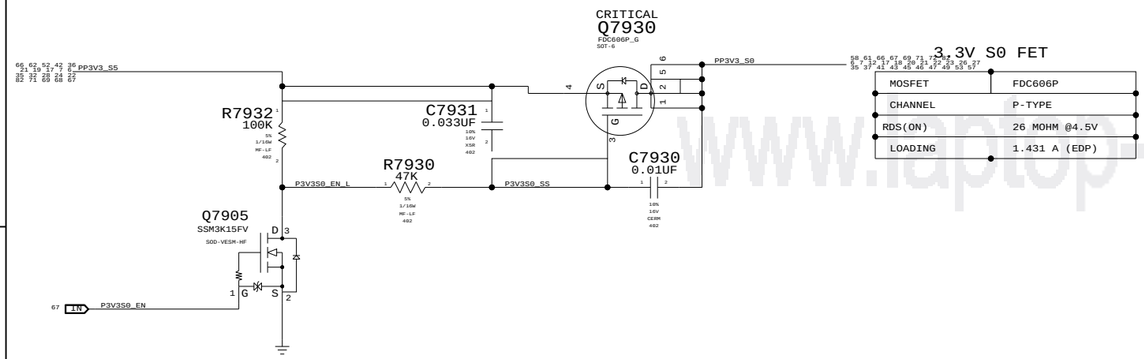
3.3V S3 FET



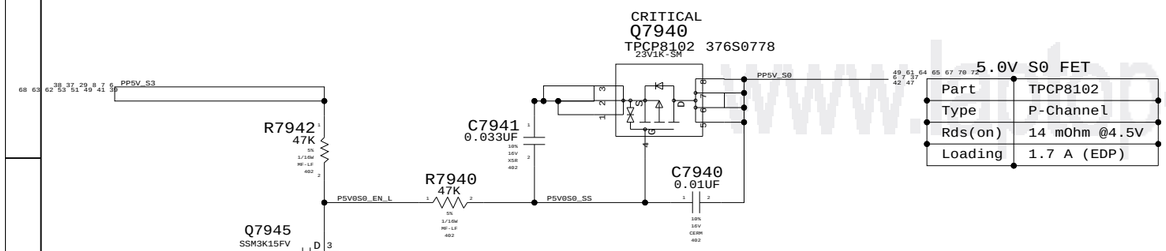
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

3.3V S0 FET



3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

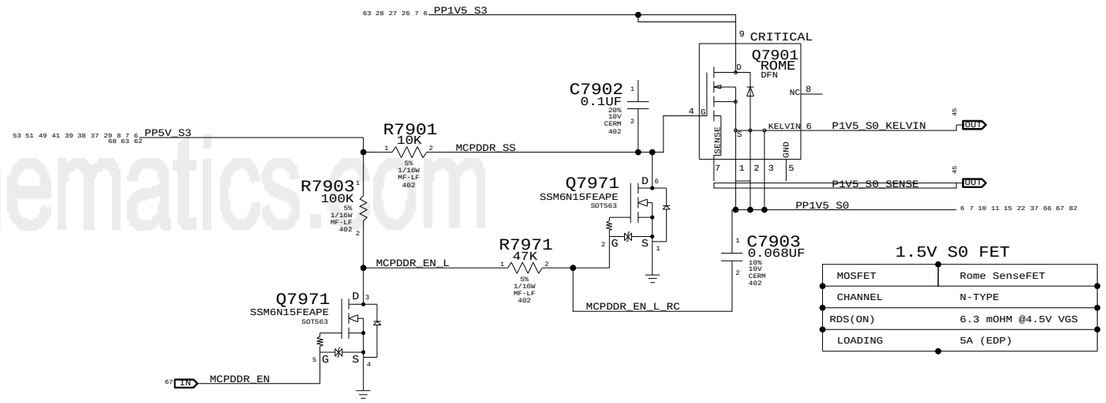
5.0V S0 FET



5.0V S0 FET	
Part	TPCP8102
Type	P-Channel
Rds(on)	14 mOhm @4.5V
Loading	1.7 A (EDP)

1.5V S0 FET

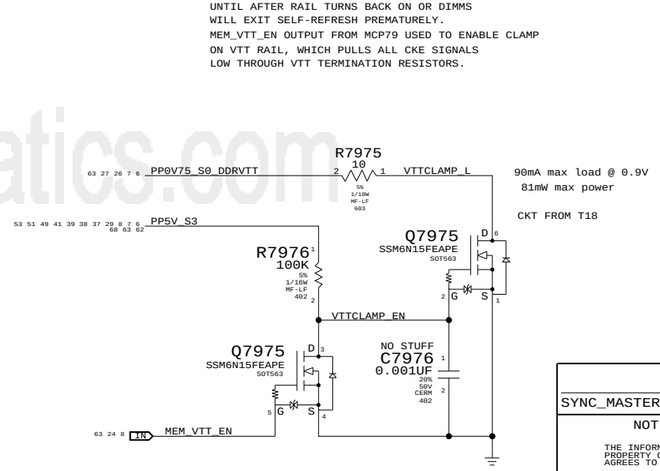
(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)



1.5V S0 FET	
MOSFET	Rome SenseFET
CHANNEL	N-TYPE
RDS(ON)	6.3 mOHM @4.5V VGS
LOADING	5A (EDP)

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



POWER FETS

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SCALE	SHT	OF
NONE	68	83

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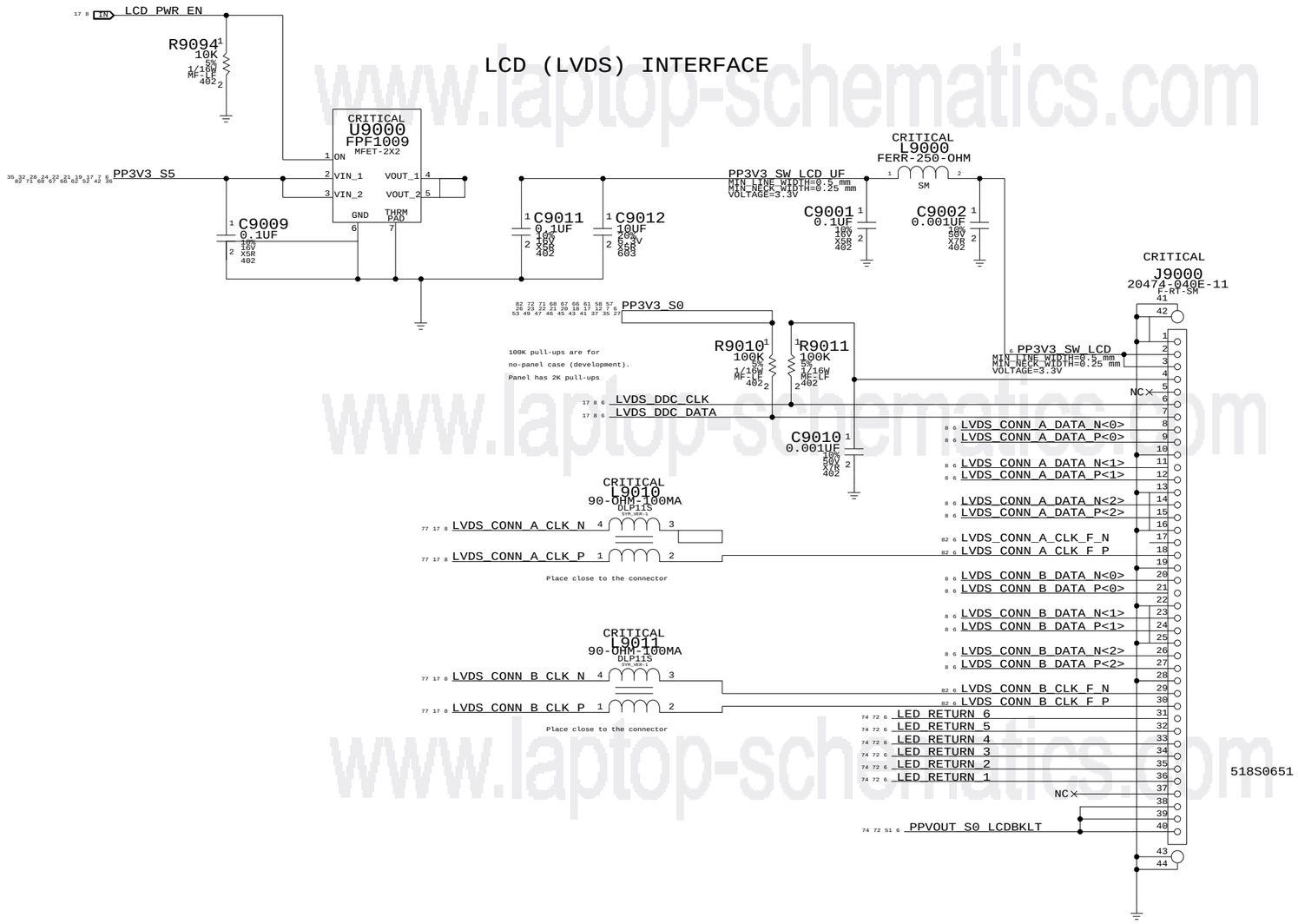
LCD (LVDS) INTERFACE



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LVDS Display Connector

SYNC_MASTER=K19_MLB SYNC_DATE=02/05/2009

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17 =MCP_HDMI_TXC_P — DP_ML_P<3> — 71 82 MAKE_BASE=TRUE
17 =MCP_HDMI_TXC_N — DP_ML_N<3> — 71 82 MAKE_BASE=TRUE
17 =MCP_HDMI_TXD_P<0> — DP_ML_P<2> — 71 82 MAKE_BASE=TRUE
17 =MCP_HDMI_TXD_N<0> — DP_ML_N<2> — 71 82 MAKE_BASE=TRUE
17 =MCP_HDMI_TXD_P<1> — DP_ML_P<1> — 71 82 MAKE_BASE=TRUE
17 =MCP_HDMI_TXD_N<1> — DP_ML_N<1> — 71 82 MAKE_BASE=TRUE
82 71 70 17 _DP_ML_P<0> — DP_ML_P<0> — 17 70 71 82 MAKE_BASE=TRUE
82 71 70 17 _DP_ML_N<0> — DP_ML_N<0> — 17 70 71 82 MAKE_BASE=TRUE
71 70 17 _DP_HPD — DP_HPD — 17 70 71 MAKE_BASE=TRUE
70 17 _DP_IG_DDC_CLK — DP_IG_DDC_CLK — 17 70 MAKE_BASE=TRUE
70 17 _DP_IG_DDC_DATA — DP_IG_DDC_DATA — 17 70 MAKE_BASE=TRUE

Display Port Interoperability spec says that sources or sinks which do both DP and DVI must depend on the external adapter for pull ups on DDC lines (since DP AUX CH has 100K pull up/down on the MLB)..

DP_AUX_CH_C_N — BI 71 82

DP_IG_DDC_DATA — 70 17 BI
R9300 33 5% 1/16W MF-LF 402
C9300 0.1UF 10% 16V X5R 402 — 82 DP_AUX_CH_SW_N

DP_AUX_CH_C_P — BI 71 82

DP_IG_DDC_CLK — 70 17 BI
R9301 33 5% 1/16W MF-LF 402
C9301 0.1UF 10% 16V X5R 402 — 82 DP_AUX_CH_SW_P

SIGNAL_MODEL=DP_AUXCH_FET
Q9300 SSM6N15FEAPE SOT563
SIGNAL_MODEL=DP_AUXCH_FET
Q9300 SSM6N15FEAPE SOT563

DP_IG_AUX_CH_P — 77 17 BI
DP_IG_AUX_CH_N — 77 17 BI

PP5V_S0 — 64 61 49 47 42 37 7 6 72 68 67 65
R9302 100K 5% 1/16W MF-LF 402
R9306 1K 5% 1/16W MF-LF 402

DDC_CA_DET_LS5V_L
Q9301 SSM3K15FV SOD-VESM-HF

DP_CA_DET — 71 IN
DP_IG_CA_DET — OUT 17

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DISPLAYPORT SUPPORT

SYNC_MASTER=K24_MLB SYNC_DATE=12/19/2008

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NONE	70	83

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Port Power Switch

CRITICAL
U9480
TPS2051B
SOT23

PP3V3_S5 → IN
PM_SLP_S3_L → EN
GND
PP3V3_S0_DPILIM
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
TP_DPPWR_OC_L → OC*

C9480 10UF 20% 6.3V X5R 603
C9481 0.1UF 20% 10V CERM 402
C9485 0.1UF 20% 10V CERM 402
CRITICAL
C9486 22UF 20% 6.3V X5R CERM 603

L9400 FERR-120-OHM-3A 0603
C9400 0.01UF 20% 50V CERM 603
PP3V3_S0_DPPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

R9420 100K 5% 1/10W MF-LF 402

HDMI_CEC

R9425 1M 5% 1/16W MF-LF 402

R9403 0 NO STUFF 5% 1/16W MF-LF 402
R9413 0 NO STUFF 5% 1/16W MF-LF 402

FL9403 12-OHM-100MA TCM1210-4SM

DP_ML_P<3> → C9414 0.1uF 10% 16V X5R 402 → DP_ML_C_P<3>
DP_ML_N<3> → C9415 0.1uF 10% 16V X5R 402 → DP_ML_C_N<3>
DP_AUX_CH_C_P
DP_AUX_CH_C_N

PP3V3_S0

R9443 100K 5% 1/10W MF-LF 402
R9442 100K 5% 1/10W MF-LF 402

DP_CA_DET

Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_L_Q
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q

Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm

R9422 1M 5% 1/10W MF-LF 402
DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.

PP3V3_S0

R9445 10K 5% 1/10W MF-LF 402
R9444 10K 5% 1/10W MF-LF 402

DP_HPD

Q9441 2N7002DW-X-G SOT-363
DP_HPD_L_Q
Q9441 2N7002DW-X-G SOT-363
DP_HPD_Q

R9423 100K 5% 1/10W MF-LF 402
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

R9421 100K 5% 1/10W MF-LF 402

DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8

CRITICAL
J9400
DSPLYPRT-M97-1
F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS	
	HOT_PLUG_DETECT	GND	
	CONFIG1	ML_LANE0P	
	CONFIG2	ML_LANE0N	
	GND	GND	
	ML_LANE3P	ML_LANE1P	
	ML_LANE3N	ML_LANE1N	
	GND	GND	
	AUX_CHP	ML_LANE2P	
	AUX_CHN	ML_LANE2N	
	DP_PWR	RETURN	

SHIELD PINS

DP_ML_CONN_P<3>
DP_ML_CONN_N<3>

DP_ESD CRITICAL D9400 RCLAMP0504F SC70-6-1

DP_ESD CRITICAL D9410 RCLAMP0524P SLP2510P8

DP_ML_CONN_P<1>
DP_ML_CONN_N<1>
DP_ML_CONN_P<2>
DP_ML_CONN_N<2>

DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8

R9401 0 NO STUFF 5% 1/16W MF-LF 402
R9431 0 NO STUFF 5% 1/16W MF-LF 402

FL9401 12-OHM-100MA TCM1210-4SM

R9400 0 NO STUFF 5% 1/16W MF-LF 402
R9430 0 NO STUFF 5% 1/16W MF-LF 402

FL9400 12-OHM-100MA TCM1210-4SM

DP_ML_C_P<0> → C9410 0.1uF 10% 16V X5R 402 → DP_ML_P<0>
DP_ML_C_N<0> → C9411 0.1uF 10% 16V X5R 402 → DP_ML_N<0>
DP_ML_C_P<1> → C9412 0.1uF 10% 16V X5R 402 → DP_ML_P<1>
DP_ML_C_N<1> → C9413 0.1uF 10% 16V X5R 402 → DP_ML_N<1>
DP_ML_C_P<2> → C9416 0.1uF 10% 16V X5R 402 → DP_ML_P<2>
DP_ML_C_N<2> → C9417 0.1uF 10% 16V X5R 402 → DP_ML_N<2>

FL9402 12-OHM-100MA TCM1210-4SM

R9402 0 NO STUFF 5% 1/16W MF-LF 402
R9432 0 NO STUFF 5% 1/16W MF-LF 402

DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8

DisplayPort Connector

SYNC_MASTER=K19_MLB SYNC_DATE=02/05/2009

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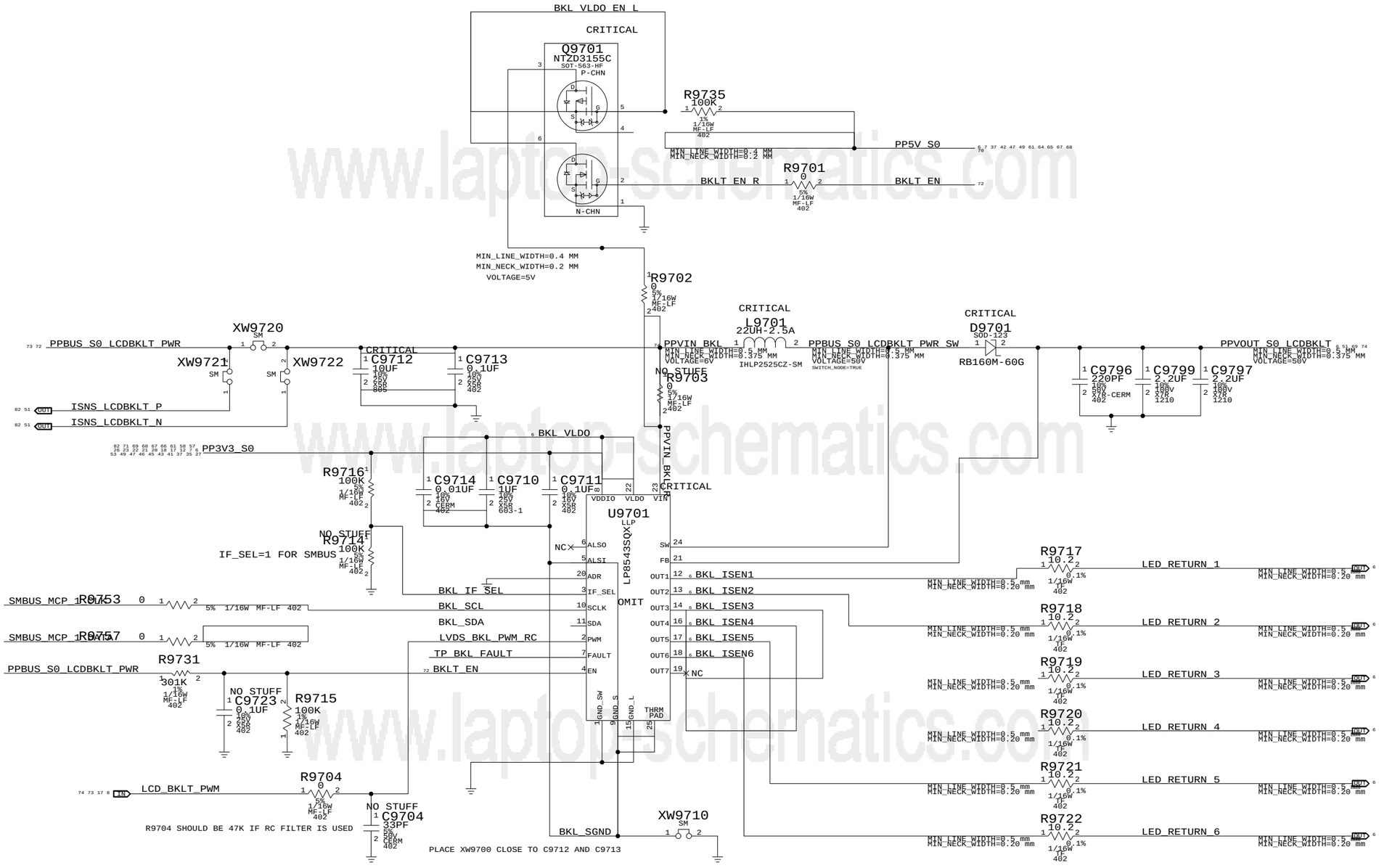
SCALE	SHT	OF
NONE	71	83

*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
* LVDS_IG_BKL_PWM SHOULD BE AWAY FROM BOOST CIRCUIT



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2670	1	IC,LP8543,WHT LED BKLT,PROD	U9701	CRITICAL	

LCD BACKLIGHT DRIVER

SYNC_MASTER=K19_MLB SYNC_DATE=02/10/2009

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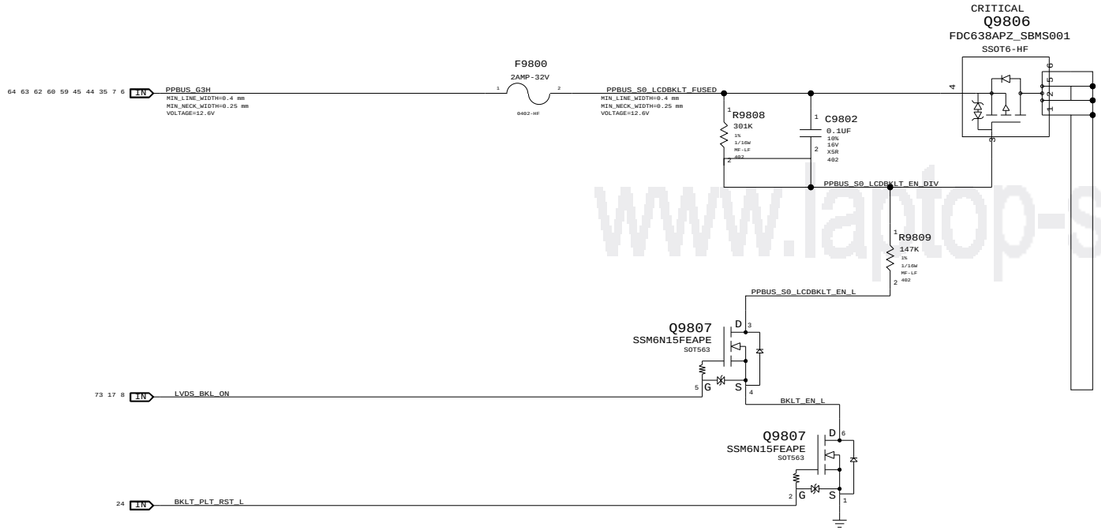

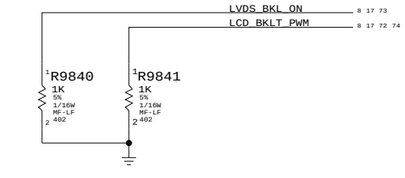

MCP HAS INTERNAL 10K PULL-UP FOR THESE SIGNALS

www.laptop-schematics.com

LCD Backlight Support

SYNC_MASTER=K24_MLB SYNC_DATE=03/16/2009

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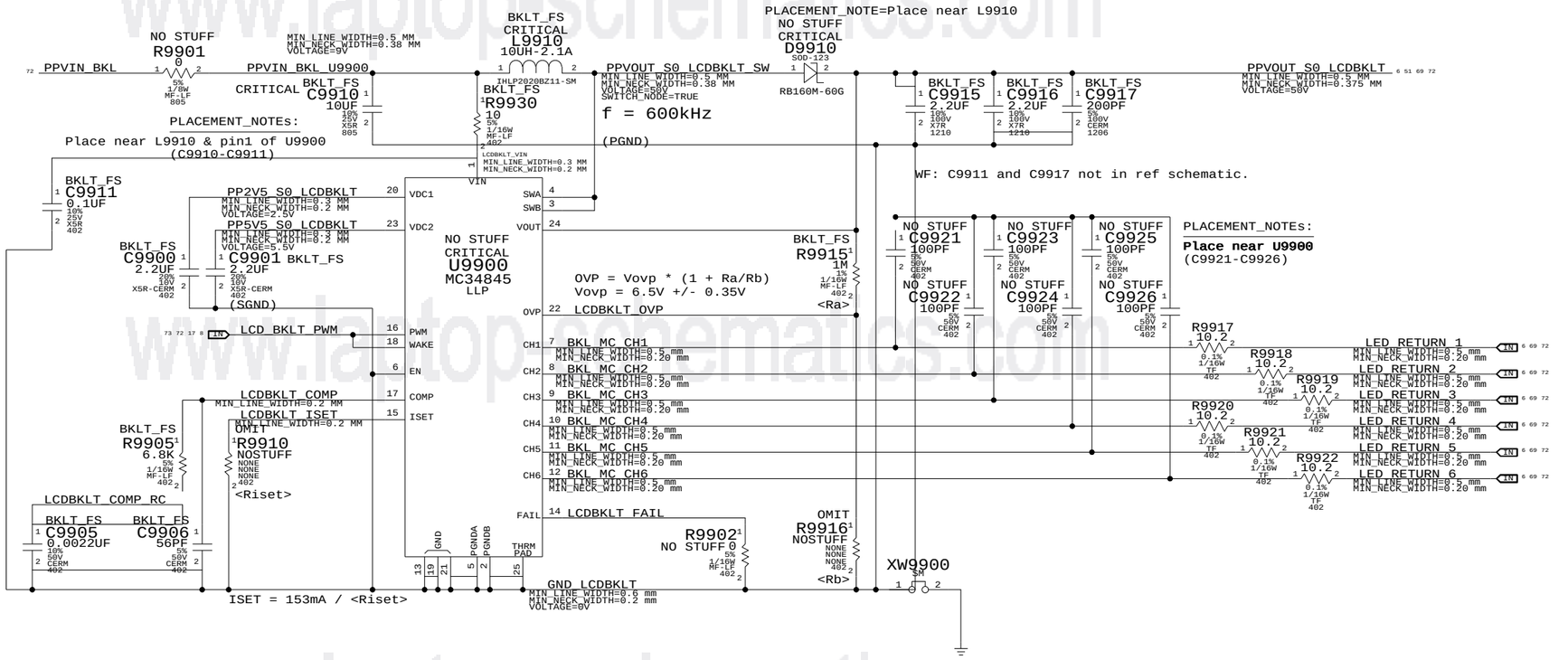

13.3 Inch Panel (9 LEDs per string)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
114S0298	1	RES,MTL FILM,1/16W,6.65K,1,0402,SMD,LF	R9910	?	LCD_13INCH	WF: Need 6.65K 0.1% resistor?
114S0445	1	RES,MTL FILM,1/16W,226K,1,0402,SMD,LF	R9916	?	LCD_13INCH	

Target: ISET = 23mA, OVP = 35V
Actual: ISET = 23mA, OVP = 35.2V

15.4 Inch Panel (10/11 LEDs per string)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
114S0298	1	RES,MTL FILM,1/16W,6.65K,1,0402,SMD,LF	R9910	?	LCD_15INCH	WF: Need 6.65K 0.1% resistor?
114S0438	1	RES,MTL FILM,1/16W,191K,1,0402,SMD,LF	R9916	?	LCD_15INCH	

Target: ISET = 23mA, OVP = 40V
Actual: ISET = 23mA, OVP = 40.5V

17 Inch Panel (14 LEDs per string)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
114S0299	1	RES,MTL FILM,1/16W,6.81K,1,0402,SMD,LF	R9910	?	LCD_17INCH	WF: Need 6.80K 0.1% resistor?
114S0428	1	RES,MTL FILM,1/16W,150K,1,0402,SMD,LF	R9916	?	LCD_17INCH	

Target: ISET = 22.5mA, OVP = 50V
Actual: ISET = 22.47mA, OVP = 49.8V

LCD Backlight Driver (MC34845)

SYNC_MASTER=VEMURI_K19I SYNC_DATE=02/09/2009

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D	051-7903	A
SCALE: NONE	SHT 74 OF 83	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	NET_TYPE		
	ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0> 6 9 13
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0> 6 9 13
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0> 6 9 13
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0> 6 9 13
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16> 6 9 13
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1> 6 9 13
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1> 6 9 13
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1> 6 9 13
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32> 6 9 13
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2> 6 9 13
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2> 6 9 13
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2> 6 9 13
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48> 6 9 13
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3> 6 9 13
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3> 6 9 13
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3> 6 9 13
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3> 6 9 13
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0> 6 9 13
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0> 6 9 13
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17> 6 9 13
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1> 6 9 13
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L 6 9 13
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L 9 13
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L 13
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L 9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L 9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L 9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L 9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L 9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L 6 9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L 6 9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L 6 9 13
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L 9 12 13
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0> 9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L 9 13
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L 9 13
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0> 8 9
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L 9 13
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L 9 13
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L 9 13
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR 9 13
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI 9 13
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L 9 13 41 61
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD 9 12 13
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L 9 13
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L 9 13
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L 9 13 41
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L 9 13
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L 9 13
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L 9 13 61
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L 9 13
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD 13
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND 13
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC 13
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND 13
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P 9 13
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N 9 13
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P 12 13
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N 12 13
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P 13
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N 13
	CPU_IERR_L	CPU_50S		CPU_IERR_L 9
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR 20 61
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR 61
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF 9 25
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3> 9
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2> 9
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1> 9
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0> 9
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI 9 12
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO 1 9 12
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS 9 12
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK 9 12
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L 9 12
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0> 9 12
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5> 9 12
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L 12
		CPU_50S	CPU_8MIL	CPU_VID<6..0> 8 10
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0> 8 61
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P 10 61
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N 10 61
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P 61
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N 61

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CPU/FSB Constraints

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE: NONE	SHT 75 OF 83	

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 1 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	14 26
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	14 26
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	14 26
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	14 26
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	14 26
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	14 26
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	14 26
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	14 26
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	14 26
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	14 26
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	14 26
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	14 26
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	14 26
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	14 26
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	14 26
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	14 26
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	14 26
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	14 26
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	14 26
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	14 26
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	14 26
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	14 26
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	14 26
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	14 26
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	14 26
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	14 26
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	14 26
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	14 26
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	14 26
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	14 26
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	14 26
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	14 26
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	14 26
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	14 26
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	14 26
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	14 26
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	14 26
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	14 26
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	14 26
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	14 26
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	14 26
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	14 26
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	14 27
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	14 27
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	14 27
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	14 27
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	14 27
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	14 27
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	14 27
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	14 27
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	14 27
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	14 27
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	14 27
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	14 27
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	14 27
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	14 27
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	14 27
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	14 27
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	14 27
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	14 27
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	14 27
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	14 27
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	14 27
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	14 27
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	14 27
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	14 27
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	14 27
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	14 27
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	14 27
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	14 27
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	14 27
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	14 27
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	14 27
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	14 27
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	14 27
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	14 27
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	14 27
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	14 27
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	14 27
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	14 27
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	14 27
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	14 27
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	14 27
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	14 27
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	15
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	15

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Memory Constraints

SYNC_MASTER=T18_MLB SYNC_DATE=02/05/2009

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7903	A

SCALE	SHT	OF
NONE	76	83

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	6 29 82
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	6 29 82
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	16 29
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	16 29
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	6 16 29
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	6 16 29
	PCIE_90D	PCIE	PCIE_FW_R2D_P	34
	PCIE_90D	PCIE	PCIE_FW_R2D_N	34
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	16 34
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	16 34
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	16 34
	PCIE_90D	PCIE	PCIE_FW_D2R_N	16 34
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	34
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	34
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P	
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N	
PCIE_EXCARD_R2D	PCIE_90D	PCIE	NC_PCIE_EXCARD_R2DCP	8 16
	PCIE_90D	PCIE	NC_PCIE_EXCARD_R2DCN	8 16
PCIE_EXCARD_D2R	PCIE_90D	PCIE	NC_PCIE_EXCARD_D2RP	8 16
	PCIE_90D	PCIE	NC_PCIE_EXCARD_D2RN	8 16
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	NC_PEG_CLK100MP	8 16
	CLK_PCIE_100D	CLK_PCIE	NC_PEG_CLK100MN	8 16
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	16 29
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	16 29
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	16 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	16 34
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	NC_PCIE_CLK100M_EXCARDP	8 16
	CLK_PCIE_100D	CLK_PCIE	NC_PCIE_CLK100M_EXCARDN	8 16
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	16
CRT_RED	CRT_50S	CRT	NC_CRT_IG_R_C_PR	17 23
CRT_GREEN	CRT_50S	CRT	NC_CRT_IG_G_Y_Y	17 23
CRT_BLUE	CRT_50S	CRT	NC_CRT_IG_B_COMP_PB	17 23
CRT_SYNC	CRT_50S	CRT_SYNC	NC_CRT_IG_HSYNC	17 23
CRT_SYNC	CRT_50S	CRT_SYNC	NC_CRT_IG_VSYNC	17 23
MCP_DAC_RSET		MCP_DAC_COMP	NC_MCP_TV_DAC_RSET	17 23
MCP_DAC_VREF		MCP_DAC_COMP	NC_MCP_TV_DAC_VREF	17 23
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0>	
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	17 70
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	17 70
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	17 23
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	17 23
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_CONN_A_CLK_P	8 17 69
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_CONN_A_CLK_N	8 17 69
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	8 17
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	8 17
LVDS_IG_A_DATA3	LVDS_100D	LVDS	NC_LVDS_IG_A_DATAP<3>	8 17
LVDS_IG_A_DATA3	LVDS_100D	LVDS	NC_LVDS_IG_A_DATAN<3>	8 17
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_CONN_B_CLK_P	8 17 69
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_CONN_B_CLK_N	8 17 69
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	8 17
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	8 17
LVDS_IG_B_DATA3	LVDS_100D	LVDS	NC_LVDS_IG_B_DATAP<3>	8 17
LVDS_IG_B_DATA3	LVDS_100D	LVDS	NC_LVDS_IG_B_DATAN<3>	8 17
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	17 23
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	17 23
SATA_HDD_R2D	SATA_100D	SATA	SATA_HDD_R2D_C_P	19 37
	SATA_100D	SATA	SATA_HDD_R2D_C_N	19 37
	SATA_100D	SATA	SATA_HDD_R2D_P	6 37
	SATA_100D	SATA	SATA_HDD_R2D_N	6 37
SATA_HDD_D2R	SATA_100D	SATA	SATA_HDD_D2R_P	19 37
	SATA_100D	SATA	SATA_HDD_D2R_N	19 37
	SATA_100D	SATA	SATA_HDD_D2R_C_P	6 37
	SATA_100D	SATA	SATA_HDD_D2R_C_N	6 37
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	19 37
	SATA_100D	SATA	SATA_ODD_R2D_C_N	19 37
	SATA_100D	SATA	SATA_ODD_R2D_P	6 37
	SATA_100D	SATA	SATA_ODD_R2D_N	6 37
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	19 37
	SATA_100D	SATA	SATA_ODD_D2R_N	19 37
	SATA_100D	SATA	SATA_ODD_D2R_C_P	6 37
	SATA_100D	SATA	SATA_ODD_D2R_C_N	6 37
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	19

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MCP Constraints 1

SYNC_MASTER=T18_MLB SYNC_DATE=02/05/2009

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7903	A

SCALE	SHT	OF
NONE	77	83

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	12 18
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI_PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	
PCI_REQ0_I	PCI_55S	PCI	PCI_REQ0_L	18
PCI_GNT0_I	PCI_55S	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	18
PCI_GNT1_I	PCI_55S	PCI	PCI_GNT1_L	
PCI_INTW_I	PCI_55S	PCI	PCI_INTW_L	
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L	
PCI_INTY_I	PCI_55S	PCI	PCI_INTY_L	
PCI_INTZ_I	PCI_55S	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	18
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	18
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	18 40 42
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	18 40 42
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	18 24
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	18 24
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	24 40
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	24 42
USB_EXTA	USB_90D	USB	USB_EXTA_P	19 38
	USB_90D	USB	USB_EXTA_N	19 38
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	NC_USB_MINIP	8 19
	USB_90D	USB	NC_USB_MININ	8 19
USB_EXTD	USB_90D	USB	NC_USB_EXTDP	8 19
	USB_90D	USB	NC_USB_EXTDN	8 19
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	6 19 29
	USB_90D	USB	USB_CAMERA_N	6 19 29
USB_BT	USB_90D	USB	USB_BT_P	6 19 29
	USB_90D	USB	USB_BT_N	6 19 29
USB_TPAD	USB_90D	USB	USB_TPAD_P	19 48
	USB_90D	USB	USB_TPAD_N	19 48
USB_IR	USB_90D	USB	USB_IR_P	19 39
	USB_90D	USB	USB_IR_N	19 39
USB_EXTB	USB_90D	USB	USB_EXTB_P	19 38
	USB_90D	USB	USB_EXTB_N	19 38
USB_EXCARD	USB_90D	USB	NC_USB_EXCARDP	8 19
	USB_90D	USB	NC_USB_EXCARDN	8 19
USB_EXTC	USB_90D	USB	NC_USB_EXTCP	8 19
	USB_90D	USB	NC_USB_EXTCN	8 19
USB_CARDREADER	USB_90D	USB	USB_CARDREADER_P	19 30
	USB_90D	USB	USB_CARDREADER_N	19 30
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	19
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	12 20 26 27 43
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	12 20 26 43
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	20 43 58 72
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	20 43 58 72
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	20 53
	HDA_55S	HDA	HDA_BIT_CLK_R	20
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	20 53
	HDA_55S	HDA	HDA_SYNC_R	20
HDA_RST_I	HDA_55S	HDA	HDA_RST_R_L	20
	HDA_55S	HDA	HDA_RST_L	20 53
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	20 53
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	20 53
	HDA_55S	HDA	HDA_SDOUT_R	20
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	20
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	20 24
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	24 40
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	20 42
	SPI_55S	SPI	SPI_CLK	52
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	20 42
	SPI_55S	SPI	SPI_MOSI	52
SPI_MISO	SPI_55S	SPI	SPI_MISO	20 42
	SPI_55S	SPI	SPI_MISO_R	52
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	20 42
	SPI_55S	SPI	SPI_CS0_L	

MCP Constraints 2

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NONE	78	83

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	17
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	17
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	17 32
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	31 32
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	17 31
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	17 31
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	31
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	17 31
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	31
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	17 31
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	17 31
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	17 31
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	17 31
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	17 31
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	17 31
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	17 31
	ENET_MII_55S	ENET_MII	ENET_RESET_L	17 31
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	31 33
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	31 33

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Ethernet Constraints

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SCALE: NONE	SHT 79 OF 83	

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP 34 36
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAN 34 36
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBP 34 36
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBN 34 36
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P 34 36
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N 34 36
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P 34 36
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N 34 36
Port 2 Not Used			

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FireWire Constraints

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SCALE	SHT	OF
NONE	80	83

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL 6 29 40 43 49
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA 6 29 40 43 49
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL 40 43 46
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA 40 43 46
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL 40 43 46 51
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA 40 43 46 51
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL 6 40 43 59 60
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA 6 40 43 59 60
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL 25 37 40 43
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA 25 37 40 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P 60
	1TO1_DIFFPAIR		CHGR_CSI_N 60
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P 60
	1TO1_DIFFPAIR		CHGR_CSO_N 60

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SMC Constraints

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SCALE NONE	SHT 81 OF 83	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	FSB_DSTB	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE

K19i Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	ENET_MDI_100D	ENETCONN	ENETCONN_P<3..0>	33
	ENET_MDI_100D	ENETCONN	ENETCONN_N<3..0>	33
	SATA_100D	SATA	SATA_ODD_R2D_UF_P	37
	SATA_100D	SATA	SATA_ODD_R2D_UF_N	37
	SATA_100D	SATA	SATA_ODD_D2R_UF_P	6 37
	SATA_100D	SATA	SATA_ODD_D2R_UF_N	6 37
	SATA_100D	SATA	SATA_HDD_R2D_UF_P	37
	SATA_100D	SATA	SATA_HDD_D2R_UF_N	37
	SATA_100D	SATA	SATA_HDD_D2R_UF_P	37
	SATA_100D	SATA	SATA_HDD_R2D_UF_N	37
CPUTHMSNS_D2	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	46
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	46
CPU_THERMD	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 46
	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 46
MCPTHMSNS_D2	THERM_1TO1_55S	THERM	MCPTHMSNS_D2_P	46
	THERM_1TO1_55S	THERM	MCPTHMSNS_D2_N	46
MCP_THMDIODE	THERM_1TO1_55S	THERM	MCP_THMDIODE_P	20 46
	THERM_1TO1_55S	THERM	MCP_THMDIODE_N	20 46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	51 63
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	51 63
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_P	51
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_N	51
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	29 51
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	29 51
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	51
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	51
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	37 51
	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	37 51
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	51
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	51
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	51 72
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	51 72
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_R_P	
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_R_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	37 51
	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	37 51
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	51
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	51
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPUVTT_P	45
	SENSE_1TO1_55S	SENSE	ISNS_CPUVTT_N	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	MCPCORES0_RSEN_P	64
	SENSE_1TO1_55S	SENSE	MCPCORES0_RSEN_N	64
		SB_POWER	PP3V3_S5	68 69 71 6 7 17 19 21 22 24 28 32 35 36 42 52 62 66 67
		SB_POWER	PP3V3_S0	6 7 12 17 18 20 21 22 23 26 27 35 37 41 43 45 46 47 49 53 57 58 61 66 67 68 69 71 72
		SB_POWER	PP1V5_S0	6 7 10 11 15 22 37 66 67 68
		GND	GND	

K19i Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	6 29 77
(PCIE_MINI)	PCIE_90D	PCIE	PCIE_MINI_R2D_N	6 29 77
(PCIE_MINI)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	6 29
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	6 29
	1TO1_DIFFPAIR		CHGR_CSI_R_P	60
	1TO1_DIFFPAIR		CHGR_CSI_R_N	60
	1TO1_DIFFPAIR		CHGR_CSO_R_P	45 60
	1TO1_DIFFPAIR		CHGR_CSO_R_N	45 60
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P	38
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N	38
(USB_EXTA)	USB_90D	USB	USB2_LT1_P	38
(USB_EXTA)	USB_90D	USB	USB2_LT1_N	38
(USB_TPAD)	USB_90D	USB	USB_TPAD_R_P	48
(USB_TPAD)	USB_90D	USB	USB_TPAD_R_N	48
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_P	6 29
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_N	6 29
	USB_90D	USB	CONN_USB2_BT_P	6 29
	USB_90D	USB	CONN_USB2_BT_N	6 29
	USB_90D	USB	USB_LT2_P	38
	USB_90D	USB	USB_LT2_N	38
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P	70
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N	70
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	6 56 57
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	6 56 57
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P	6 56 57
	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N	6 56 57
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	6 56 57
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	6 56 57
	DIFFPAIR	AUDIO	SPKRAMP_L_OUT_P	56
	DIFFPAIR	AUDIO	SPKRAMP_L_OUT_N	56
	DIFFPAIR	AUDIO	SPKRAMP_R_OUT_P	56
	DIFFPAIR	AUDIO	SPKRAMP_R_OUT_N	56
	DIFFPAIR	AUDIO	SPKRAMP_S_OUT_P	56
	DIFFPAIR	AUDIO	SPKRAMP_S_OUT_N	56

K19i Specific Graphics Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_P	6 69
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_N	6 69
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_P	6 69
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_N	6 69
DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	6 71
	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	71
DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	17 70 71
	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	17 70 71
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	71
	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	71
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	70 71
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	70 71

SD Card Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
SD_DATA	SD_55S	SD_INTERFACE	SD_D<0>	6 30
SD_DATA	SD_55S	SD_INTERFACE	SD_D<1>	6 30
SD_DATA	SD_55S	SD_INTERFACE	SD_D<2>	6 30
SD_DATA	SD_55S	SD_INTERFACE	SD_D<3>	6 30
SD_DATA	SD_55S	SD_INTERFACE	SD_D<4>	6 30
SD_DATA	SD_55S	SD_INTERFACE	SD_D<5>	6 30
SD_DATA	SD_55S	SD_INTERFACE	SD_D<6>	6 30
SD_DATA	SD_55S	SD_INTERFACE	SD_D<7>	6 30
SD_CLK	SD_55S	SD_INTERFACE	SD_CLK	6 30
SD_CMD	SD_55S	SD_INTERFACE	SD_CMD	6 30

SD Card Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

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K19i Specific Constraints

SYNC_MASTER=WFERRY_K19I SYNC_DATE=01/08/2009

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A

SCALE	SHT	OF
NONE	82	83

K19i Board-Specific Physical & Spacing Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.080 MM	12.7 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.151 MM	0.151 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF_HDD	ISL3,ISL4,ISL9,ISL10	Y	0.083 MM	0.083 MM		0.400 MM	0.400 MM
100_OHM_DIFF_HDD	TOP,BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?
5X_DIELECTRIC	*	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_LPC	*	BGA	BGA_P2MM
CLK_PCI	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA	STANDARD
MEM_40S_VDD	BGA	STANDARD

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K19i PCB Rule Definitions

SYNC_MASTER=WFERRY_K19I SYNC_DATE=12/12/2008

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